Application Report
SNLA112E–October 2008–Revised April 2013

AN-1909 DS15BA101 and DS15EA101 Enable Long Reach Applications for Embedded Clock SER/DES

ABSTRACT

Reduction in system size, increase in system performance and savings in system cost are valuable benefits that SER/DES devices (Serializers and Deserializers) bring to many system designers. These benefits are the reason why SER/DES are integral pieces of many of today's high-speed systems. One of the design constraints for these systems is the maximum transmission distance between a serializer and a deserializer. While most SER/DES can support transmission over only several meters of cable, many systems require the transmission distance between a serializer and a deserializer to be tens and even hundreds of meters. This application report introduces the DS15BA101 and DS15EA101, a cable extender chipset, which can enable long reach applications for SER/DES devices. It also lists Texas Instruments SER/DES that can benefit from the chipset, discusses distance limitations of the SER/DES and the distance gains that can be realized with the aid of the chipset in applications utilizing both single-ended and differential interconnects.

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1 Cable Extender Chipset Overview

The cable extender chipset consists of the DS15BA101 and DS15EA101 devices. These are flexible devices that can be used with LVDS, LVPECL or CML signaling and establish links over single-ended (for example, coaxial cables) and differential (for example, twisted pair cables) media.

The DS15BA101 is a high-speed differential buffer with adjustable output amplitude. It can be used for cable driving, level translation, signal buffering and signal repeating. It operates from DC to 1.5+ Gbps. Its wide input common mode voltage range allows for a DC-coupled interface to most SER drivers (CML, LVDS, LVPECL).

The DS15EA101 is an adaptive equalizer optimized for equalizing data transmitted over coaxial and differential balanced copper cables. The operating range for the equalizer is from 150 Mbps to 1.5+ Gbps. It automatically equalizes any cable length from zero meters to lengths that attenuate the signal by approximately –35 dB at 750 MHz. The cables may be differential (for example, twisted pair cables) or single ended (for example, coaxial). Figure 1 shows a typical application of the chipset. Note the three important eye pattern locations in the example application. The serial signal is repeated and level shifted by the DS15BA101. The eye pattern at this location has optimal launch amplitude and very low jitter. After the losses due to the long cable, the eye pattern is essentially closed. The signal amplitude is attenuated and jitter is excessive. The DS15EA101 provides gain that compensates for the cable losses, maintains the DC-balance of the data, and also repeats and level shifts the recovered eye pattern. Jitter is greatly reduced, and the signal amplitude is also recovered.

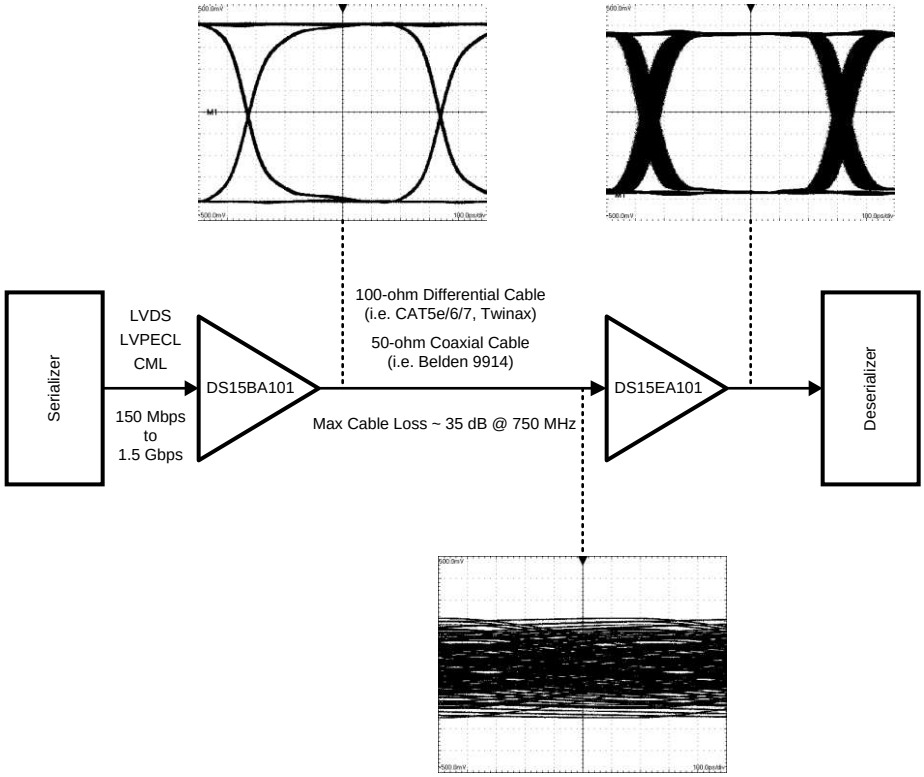

Figure 1. Typical Cable Extender Chipset Application

It is important to realize that the performance of the DS15EA101's automatic equalization circuitry is dependant on the signal amplitude at the transmitter or cable driver end of the cable, known as the launch amplitude. For 100Ω differential cables (twin-axial or twisted pair cables), the optimal launch amplitude is ±400 mV (800 mV peak-peak or differential); and for 50Ω coaxial cables it is 800 mV single-ended (V_{OH}–V_{OL}). The energy detector circuitry in the DS15EA101 quantifies the energy of the incoming signal and feeds this analog information to the automatic equalization control circuitry which compares it with the assumed energy of the original signal and instructs the equalizer filter to apply certain amount of gain to the high frequency components of the signal based on the comparison. Any deviation from the optimal

launch amplitude in either direction will cause the equalizer filter to assert either excessive or insufficient amount of gain as illustrated in Figure 2. The DS15BA101 can provide signals with optimal launch amplitude for equalization of both, differential and single-ended cables with minimal deviation over process, voltage and temperature. This is the reason why the serializer driver needs to be buffered by the DS15BA101 in the example of Figure 1.

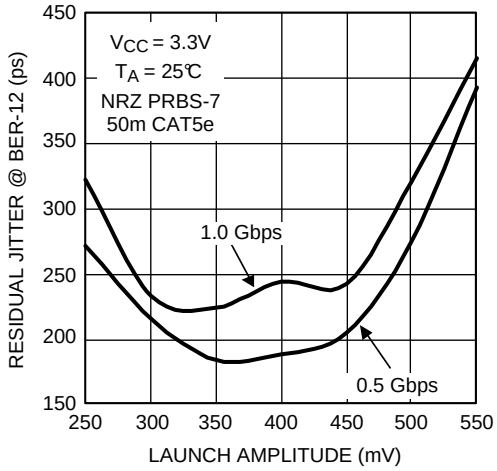

Figure 2. DS15EA101 Output Residual Jitter as a Function of Launch Amplitude

Figure 2 shows how the launch amplitude affects the DS15EA101 output residual jitter when equalizing a 50m CAT5e cable. It is clear that having launch amplitude that is smaller or larger than the optimal amplitude (±400 mV for 100Ω differential cables) results in a higher output residual jitter. The data provided in Figure 2 was measured using a single twisted pair of the 50m CAT5e cable. The other twisted pairs in the cable were doubly terminated with 100Ω resistors to minimize reflections and crosstalk.

2 SER/DES that can Benefit from the Cable Extender Chipset

While any SER/DES chipset that transmits/receives serialized binary data that is within the 0.15 Gbps to 1.5 Gbps range may benefit from the cable extender chipset, SER/DES that operate with a single high-speed serial DC-balanced data stream (for example, Embedded Clock SER/DES) are best suited for coupling with the cable extender chipset. SER/DES that operate with multiple serial data and clock streams (for example, Parallel Clock SER/DES) may also benefit from the cable extender chipset, however, these SER/DES typically run into channel-to-channel skew issues before they encounter cable attenuation problems. Table 1 lists selected Texas Instruments SER/DES that may be coupled with the cable extender chipset. For the full list of currently available SER/DES, visit ti.com.

Table 1. Selected SER/DES that can Benefit from the Cable Extender Chipset

SER/DES Chipset	Clock Frequency Range	Raw Serial Data Rate Range
10-Bit B-LVDS Embedded Clock SER/DES		
DS92LV1021A / DS92LV1212A	16 MHz–40 MHz	192 Mbps–480 Mbps
DS92LV1023E / DS92LV1224	30 MHz–66 MHz	360 Mbps–792 Mbps
SCAN921025H / SCAN921226H	20 MHz–80 MHz	240 Mbps–960 Mbps
16-Bit and 18-bit B-LVDS Embedded Clock SER/DES		
DS92LV16	25 MHz–80 MHz	450 Mbps–1440 Mbps
DS92LV18	15 MHz–66 MHz	300 Mbps–1320 Mbps
24-Bit FPD-Link II Embedded Clock SER/DES		
DS90C124 / DS90C241	5 MHz–35 MHz	140 Mbps–980 Mbps
DS90UR124 / DS90UR241	5 MHz–43 MHz	140 Mbps–1204 Mbps
DS99R103 / DS99R104	3 MHz–40 MHz	84 Mbps–1120 Mbps

3 SER/DES Distance Limitations

Many factors impact performance of SER/DES devices. These factors include pattern characteristics, SER/DES I/O characteristics, reference clock characteristics, connector and cable characteristics, power supply noise and system noise characteristics. While all these factors need to be carefully examined when designing systems with SER/DES, cable characteristics are typically the dominant factors that govern the distance boundaries for SER/DES devices. Depending on the cable type, key cable characteristics may be attenuation, crosstalk, and channel-to-channel skew.

Extensive empirical data collected using Texas Instruments Embedded Clock SER/DES and different cable types have shown that the SER/DES devices can handle cable loss that is between –3 dB and –6 dB at the Nyquist frequency of the raw serial data rate. For example, Figure 3 shows typical performance of the DS92LV18 when transmitting data over CAT5e cable along with the –3 dB and –6 dB curves derived purely using the cable's insertion loss characteristic. The chip is a representative of Texas Instruments B-LVDS Embedded Clock SER/DES family of products. As Figure 3 illustrates, the chip can transmit data over a single twisted pair of a CAT5e cable that is only 5–10 meters long when operating at the upper end of the operating frequency range; at the lower frequency end, the cable may be longer. Note that the data was collected under typical engineering laboratory conditions and using only a single twisted pair of a CAT5e cable. There was one DS92LV18 device transmitting and another device receiving the signal.

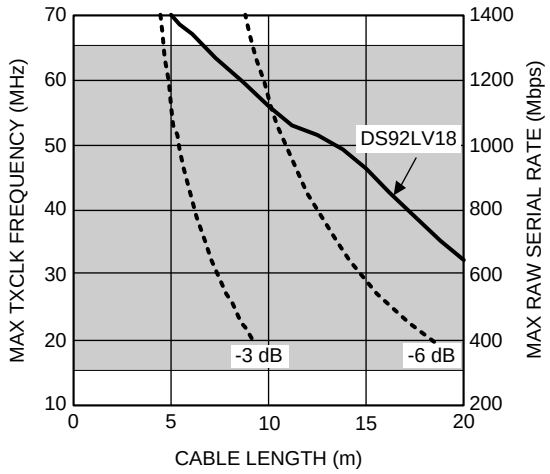

Figure 3. Typical Embedded Clock SER/DES Reach over CAT5e Cable

One can only use cable insertion loss to get a rough idea of SER/DES reach capabilities. If the insertion loss of a given cable is lower than –3 dB at Nyquist frequency, then equalization is likely not needed. All SER/DES devices from Table 1 are able to handle that much loss. If the insertion loss is between –3 dB and –6 dB, the SER/DES chipset may still be able to handle the loss depending on the transmitter clock frequency (TxCLK or PCLK), however, one may consider using some type of equalization to gain additional noise margin. If the loss is higher than –6 dB, the SER/DES link probably does not have much noise margin left and one should definitely consider using some type of cable extender solution if a longer transmission distance is needed.

For example, consider the loss characteristic of the CAT5e cable given in Figure 4 and the need for transmitting a 500 Mbps NRZ serial bit stream. For a 500 Mbps NRZ signal, Nyquist frequency is 250 MHz. The loss curve provided in Figure 4 shows that the CAT5e insertion loss at 250 MHz is approximately –0.35 dB/m. Knowing this loss per length information, it is easy to calculate that 8.5m and 17m of CAT5e introduce –3 dB and –6 dB of loss, respectively. Therefore, it can be concluded that any SER/DES chipset from Table 1 should be able to transmit a 500 Mbps raw serial data over 8.5m to 17m of CAT5e cable; however, to ensure that there is enough timing and noise margin available for reliable operation, one should consider using some type of equalization if transmission distance in excess of 8.5m is desired.

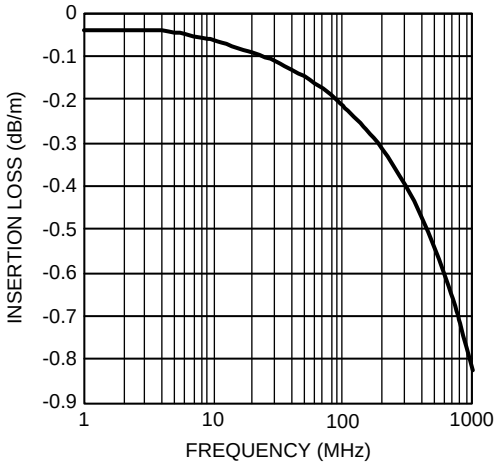

Figure 4. CAT5e Maximum Attenuation per TIA/EIA-568–B.2

Based on the data presented in this section, it is evident that the signal transmission between a serializer and a deserializer is limited to relatively short distances. The following sections show how the DS15BA101/DS15EA101 chipset can extend the transmission distance of the SER/DES and the distance gains that can be realized.

4 Extending the Reach of Embedded Clock SER/DES over Differential Balanced Cables

As the previous section has demonstrated, SER/DES devices have relatively short reach over copper cables. Applications that require longer reach may benefit from the cable extender chipset. This section of the application report shows how to design a SER/DES link with the cable extender chipset and 100Ω differential balanced cables. The application report AN-1826 specifically addresses the extension of the FPD-Link II Embedded Clock SER/DES links over CAT5e cable.

4.1 Interface Details

The 10-bit, 16-bit and 18-bit SER devices (see Table 1) output raw serial data without DC-balancing; therefore, their differential outputs need to be DC-coupled to the DS15BA101 inputs as illustrated in Figure 5. A 100Ω termination resistor placed as close to the DS15BA101 inputs as possible is all that is needed when interfacing the SER outputs to the DS15BA101 inputs. The DS15BA101 wide input common mode voltage range (1V to 3.3V) allows for a DC-coupled interface with LVDS, B-LVDS and CML drivers.

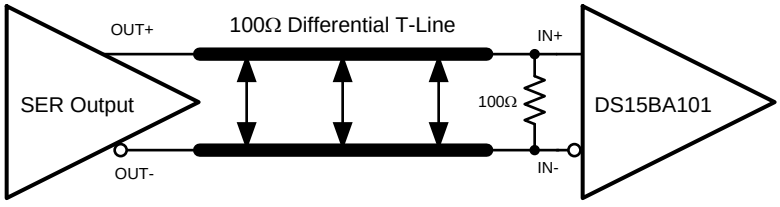

Figure 5. The 10-bit, 16-bit, and 18-bit SER Outputs Need to be DC-coupled to the DS15BA101 Inputs

In case of the 24-bit SER devices (see Table 1), the interface to the DS15BA101 input may be AC-coupled as they provide well DC-balanced raw serial data. Coupling capacitors should be 0.1 µF or greater. The example AC-coupled interface is shown in Figure 6.

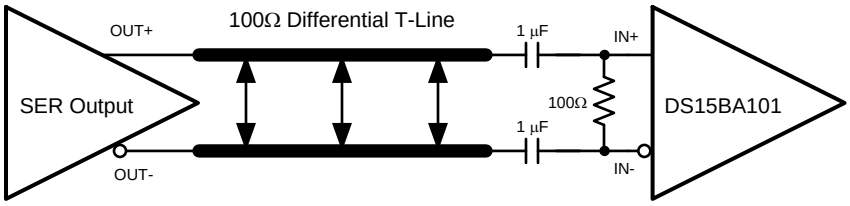

Figure 6. The 24-bit SER Outputs May be AC-coupled to the DS15BA101 Inputs

The DS15BA101 device requires an external resistor, R_{VO}, to V_{DD} to set the optimal launch amplitude. A value of 953Ω is recommended for differential 100Ω applications. The DS15BA101 outputs also require two 50Ω resistors pulled to V_{DD}. All three resistors need to have 1% or better tolerance to ensure minimal variation of the launch amplitude. The long reach cable needs to be AC-coupled at both ends to provide maximum isolation of the source and sink ends due to cable faults. The detailed connection diagram is shown in Figure 7.

The DS15EA101 device requires an external filter cap as shown and recommended in the datasheet. The DS15EA101 features built-in DC-offset correction circuitry, so even though the B-LVDS Embedded Clock SER device does not DC-balance the raw serial data, the equalizer can recover the data without errors.

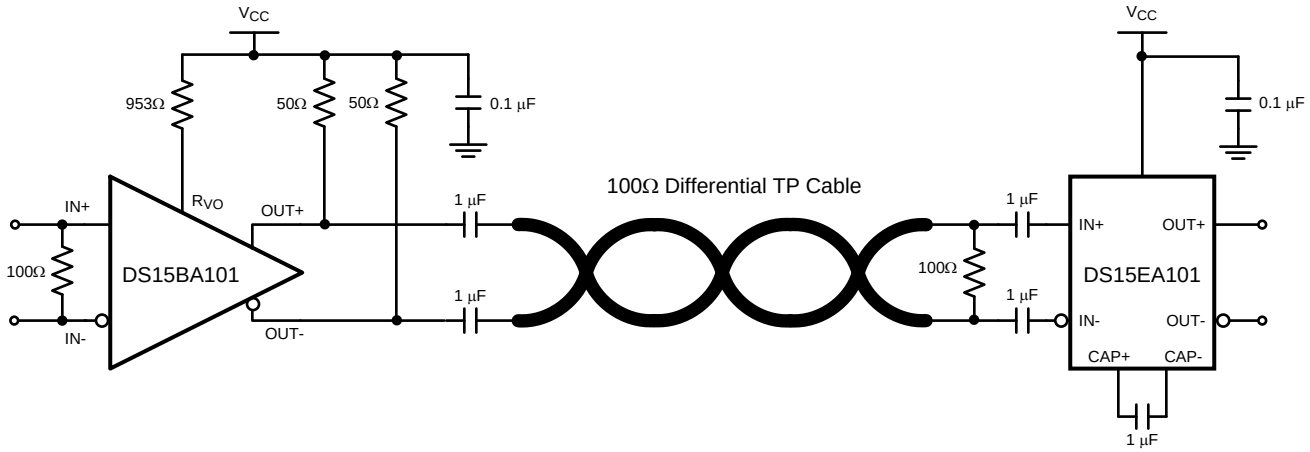

Figure 7. Cable Extender Chipset Connection Diagram for 100Ω Differential Balanced Cables

The DS15EA101 differential outputs include internal 50Ω pull up resistors. The DS15EA101 differential outputs can be DC-coupled directly to the 10-bit, 16-bit and 18-bit DES inputs as they have 0V to 3.3V input common mode voltage range. Recall that the data from their compatible SER is not DC-balanced; therefore, the DC-coupled interface to the DES device is a must. Figure 8 illustrates DC-coupled interface between the DS15EA101 output and a DES input.

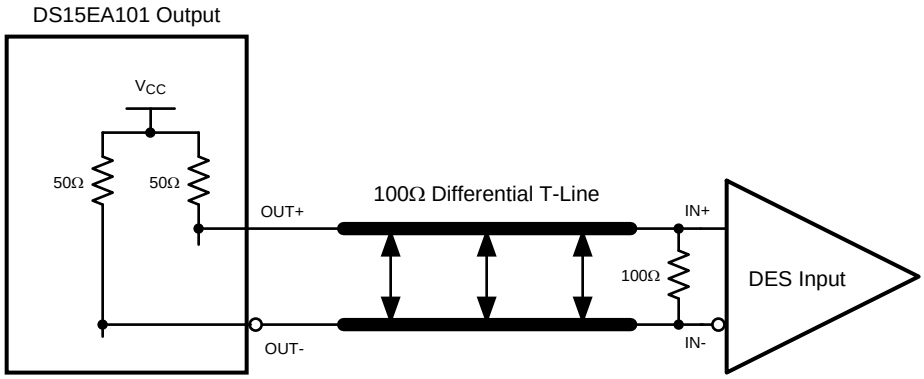

Figure 8. The DS15EA101 Outputs Need to be DC-Coupled to the 10-bit, 16-bit, and 18-bit DES Inputs

On the other side, the 24-bit DES devices do not have a wide input common mode voltage range but their compatible SER devices do output DC-balanced data, so the DS15EA101 differential outputs must be AC-coupled for compatibility reasons. The example AC-coupled interface is shown in Figure 9.

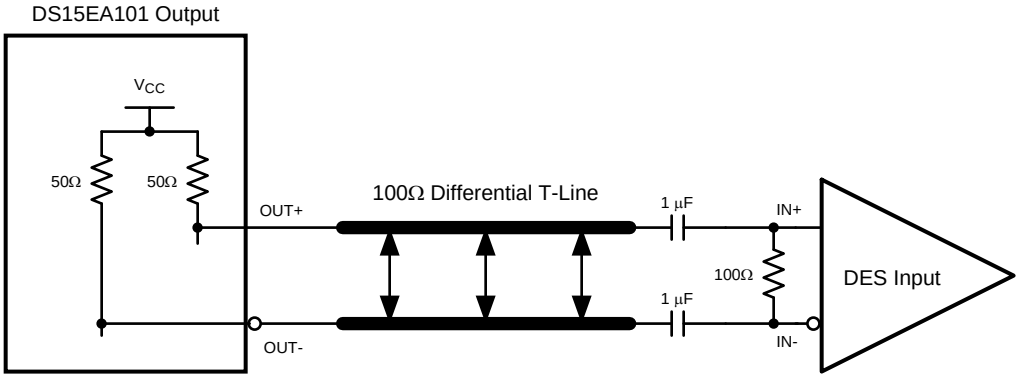

Figure 9. The DS15EA101 Outputs Need to be AC-Coupled to the 24–bit DES Inputs

The transmission line between the DS15EA101 outputs and the DES inputs needs to be terminated. The 100Ω termination should be placed as close to the DES inputs to minimize any resulting stub lengths.

4.2 Distance Gains

Extensive empirical data was collected using Texas Instruments Embedded Clock SER/DES and the cable extender chipset to show what kind of distance gains can be realized. For example, Figure 10 shows typical distance gains one can achieve with the cable extender chipset for the DS92LV18 when transmitting data over CAT5e cable.

As Figure 10 illustrates, the DS92LV18+DS15BA101/DS15EA101 solution can transmit data over a single twisted pair of a CAT5e cable that is in the excess of 100 meters long when operating at the lower frequency end. In the upper frequency band (50 MHz–66 MHz), the solution can transmit data over the distances of 25 to 50 meters. This is a 3-4 time increase in transmission distance when compared to the solution without the cable extender chipset (See Figure 3).

The empirical data in Figure 10 was collected under typical engineering laboratory conditions using the following evaluation boards: DriveCable02EVK, LVDS-18B-EVK, and DS91C176EVK. System designers should use this information as a guideline only and perform additional measurements to quantify the maximum transmission distance of SER/DES in their systems.

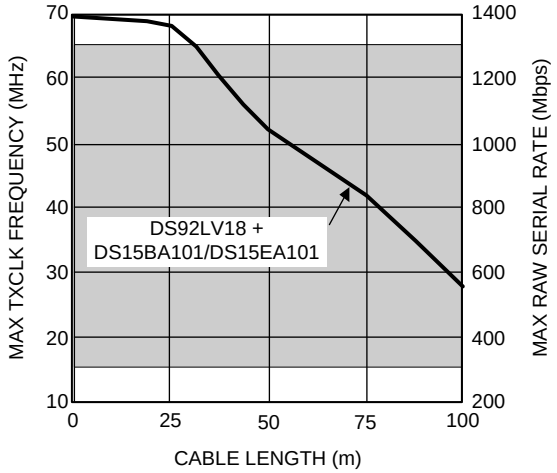

Figure 10. Typical Embedded Clock SER/DES + DS15BA101/DS15EA101 Reach over CAT5 Cable

5 Extending the Reach of Embedded Clock SER/DES over Coaxial Cables

As it was mentioned in Section 1.0, the DS15BA101/DS15EA101 chipset is able to work with both, single-ended and differential transmission media. This section of the application report shows how to design a SER/DES link with the cable extender chipset and 50Ω coaxial cables.

5.1 Interface Details

Most of the recommendations given in Section 4.1 apply to the SER/DES + DS15BA101/DS15EA101 solution with 50Ω coaxial cables as well. The major difference of the connection diagram of Figure 11 from the connection diagram of Figure 7 is the value of the R_{VO} resistor. When the R_{VO} is set to 487Ω, the DS15BA101 output provides optimal launch amplitude for the DS15EA101 when equalizing 50Ω coaxial cables. The optimal launch amplitude for equalization of 50Ω coaxial cables is 800 mV single-ended.

The only other difference is the termination network on the DS15EA101 inputs. The input that is connected to the cable is terminated with a 50Ω resistor to GND. The unused input is terminated with a 25Ω resistor to GND. This way, both DS15EA101 inputs "see" similar load. The detailed connection diagram is shown in Figure 11.

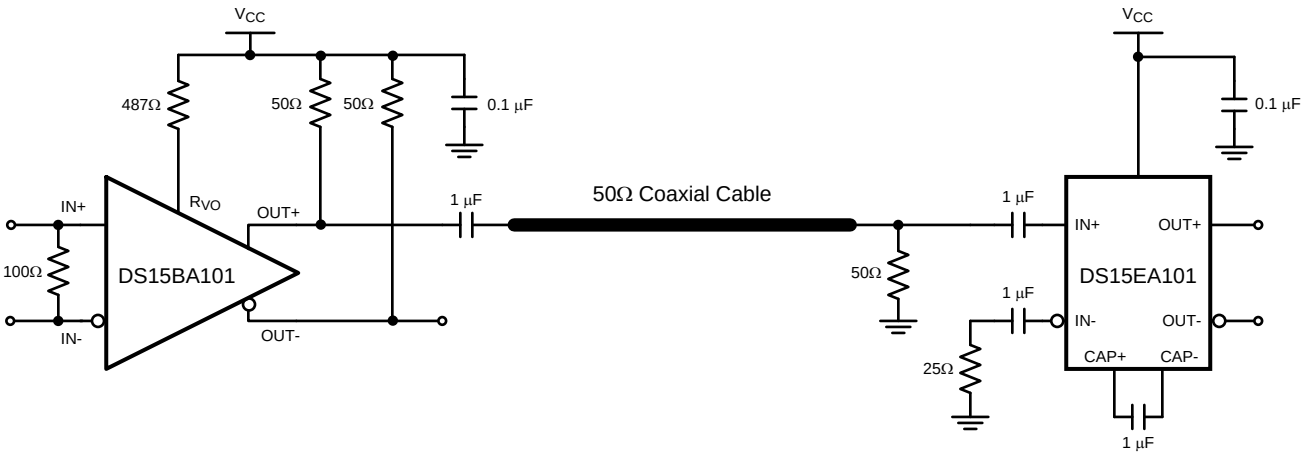

Figure 11. Cable Extender Chipset Connection Diagram for 50Ω Coaxial Cables

5.2 Distance Gains

When it comes to transmission over coaxial cables, the achievable transmission distance may vary significantly from one coaxial cable type to the other. For example, Heliax LDF6-50 by Andrew is an ultra low loss cable. Its insertion loss at 400 MHz is only –1.76 dB / 100m. This means that you can transmit an 800 Mbps NRZ signal over about 170 meters and only observe about –3 dB of loss. As the embedded clock SER/DES can tolerate the interconnect loss that is as high as –6 dB, one could transmit the signal over 340 meters without introducing some type of equalization. However, this exceptional cable performance does not come for free. Its cost alone makes it unfit for many applications. The use of the DS15BA101/DS15EA101 chipset enables similar transmission distances over more economical coaxial cables. For example, Figure 12 shows typical distance gains one can achieve with the cable extender chipset for the DS92LV18 when transmitting data over a low loss 50Ω coaxial cable (Belden 9914).

As Figure 12 illustrates, the DS92LV18+DS15BA101/DS15EA101 solution can transmit data over Belden 9914 that is in the excess of 200 meters. As the transmission over coaxial cables without the cable extender chipset is not recommended for the DS92LV18, as its high speed I/Os are differential, the maximum reach of the DS92LV18 alone over Belden 9914 was not empirically determined. However, Belden 9914 insertion loss characteristic provided in Figure 13 allows us to determine the theoretical limit. Simple calculation reveals that about 55m long Belden 9914 cable introduces –6 dB at 660 MHz (Nyquist frequency of the DS92LV18 maximum raw serial rate).

The empirical data in Figure 12 was collected under typical engineering laboratory conditions using the following evaluation boards: DriveCable02EVK and LVDS-18B-EVK.

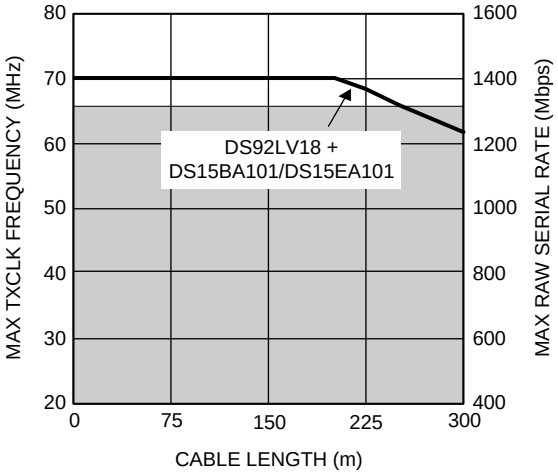

Figure 12. Typical Embedded Clock SER/DES + DS15BA101/DS15EA101 Reach over Belden 9914 (A Low Loss 50Ω Coaxial Cable)

In addition to Belden 9914 loss characteristics, Figure 13 shows the insertion loss of a couple of other standard 50Ω coaxial cables that have higher loss but are more economical: Belden 7807A (RG-58/U type) and Belden 7805 (RG-174/U type). Based on the empirical data of Figure 12 and the insertion loss characteristics of the two cables compared to the loss characteristics of Belden 9914, one can roughly estimate the transmission distance that could be achieved with the DS92LV18 + DS15BA101/DS15EA101 solution over the two cables. For example, the empirical data of Figure 12 shows that the solution can transmit a 1.2 Gbps signal (60 MHz TxCLK) over 300m Belden 9914. At Nyquist frequency of 600 MHz, the 300m Belden 9914 introduces about –30 dB of loss. This means that the solution can handle approximately –30 dB of interconnect loss. As Belden 7807A introduces approximately –0.25 dB/m at 600 MHz, it is easy to calculate that the solution can roughly handle about 120 meters of the 7807A cable. Similarly, the reach estimate for the Belden 7805 is only 50m as this is the cable with the highest insertion loss (–0.6 dB/m at 600 MHz) out of the three cables.

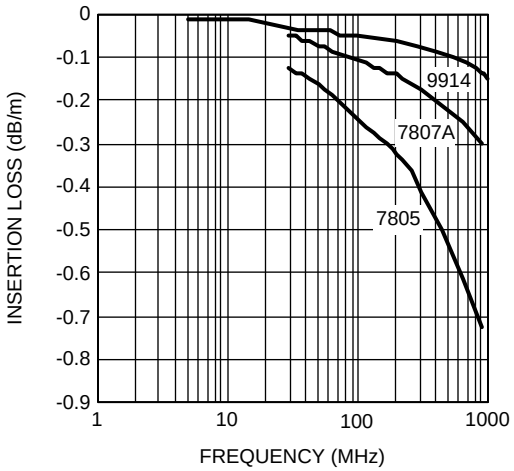

Figure 13. Attenuation of Standard 50Ω Coaxial Cables: Belden 7805 (RG-174/U, 25 AWG), Belden 7807A (RG-58/U, 17 AWG), and Belden 9914 (RG-8/U, 10 AWG)

6 Conclusion

Texas Instruments Embedded Clock SER/DES bring many benefits to system designers; however their achievable transmission distance is limited. The DS15BA101/DS15EA101 chipset not only extends the transmission distance greatly, but also enables transmission over both single-ended (for example, coaxial cables) and differential (for example, twisted pair cables) interconnects.

7 References

DS92LV18 18-Bit Bus LVDS Serializer/Deserializer 15–66 MHz (SNLS156)

DS15BA101 1.5 Gbps Differential Buffer with Adjustable Output Voltage (SNLS234)

DS15EA101 0.15 to 1.5 Gbps Adaptive Cable Equalizer with LOS Detection (SNLS235)

AN-1826 Extending the Reach of a FPD-Link II Interface with Cable Drivers and Equalizers Application Report (SNLA103)

AN-1898 LVDS Repeaters and Crosspoints Extend the Reach of FPD-Link II Interfaces Application Report (SNLA111)

AN-1347 PCB Layout Techniques for Adaptive Cable Equalizers Application Report (SNLA069)

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