Application Report
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Controlling the ADS8342 With TMS320 Series DSPs

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ABSTRACT

The ADS8342 16-bit, bipolar input, parallel output analog-to-digital converter has a number of features that allow for an easy interface to many of the TMS320™ DSP family of digital signal processors from Texas Instruments. This application note focuses on configuring, sampling, and converting analog data presented to the ADS8342 ADC, with software examples using the TMS320C6711 and C5416 DSPs. The software code developed for this application note shows how the BUSY pin of the ADC can be used as an interrupt source to the host processor. The code is available for download and contains two projects in two directories, one for each processor mentioned above. Project collateral discussed in this application note can be downloaded from the following URL: http://www.ti.com/lit/zip/SLAA176.

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1 Introduction

The ADS8342 is a multiplexed four channel, 16-bit parallel ADC, with bipolar inputs. The device features a chip select (CS), input clock (CLK), parallel data input (D [0:15]), and flexible control signals that can interface directly to the C2000™ DSP, C3000™ DSP, C5000™ DSP and C6000™ DSP platforms.

The ADS8342 operates from +/-5 volt analog (AVdd) and digital (DVdd) supplies. The device also incorporates an internal buffer that can be powered from the same 3.3-V supply as the DSP. The buffer voltage (BVdd) allows direct interfacing to 3 or 5-volt systems, eliminating the need to level shift the data and control lines.

The sample code described in Section 5 of this report was developed using *Code Composer Studio*™ V2.20 on the C6711DSK and C5416DSK with the ADS8342EVM. These simple code examples demonstrate how to configure a DSP, initialize the data converter, and process an interrupt (via the BUSY pin) from the data converter.

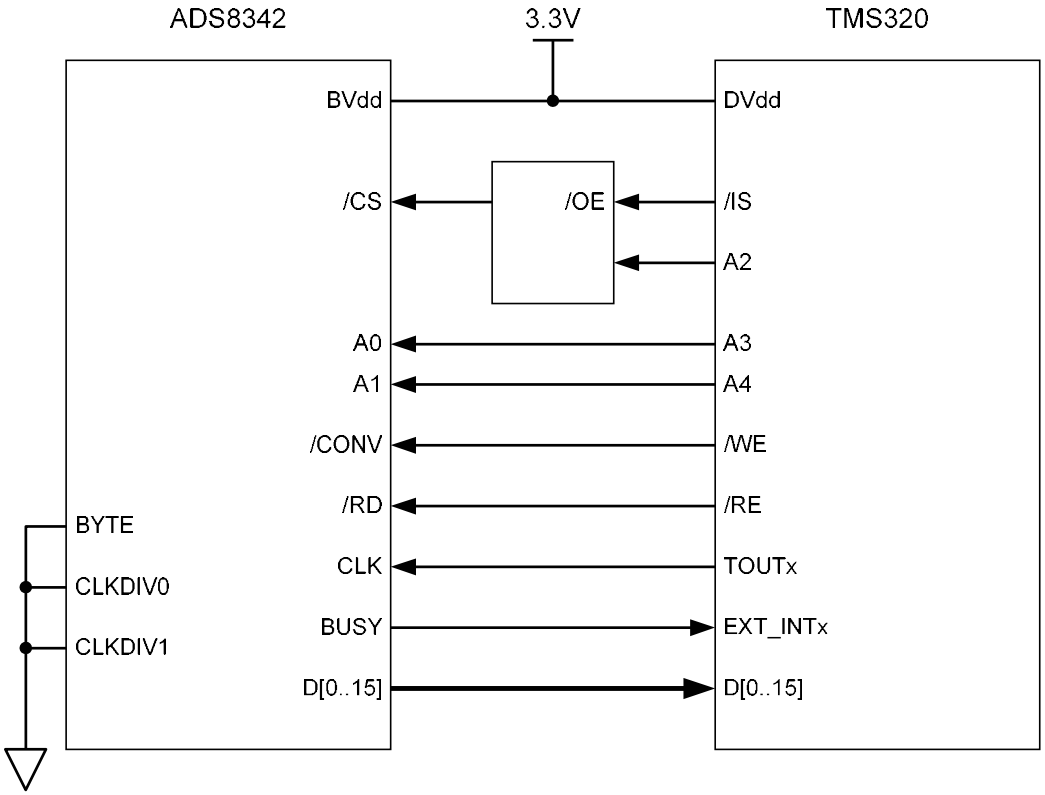

Figure 1. Typical System Block Diagram

2 The ADS8342 EVM Digital Interface

The ADS8342EVM is part of a series of *Modular EVMs* from the TI's Data Acquisition Products Group. The EVM is designed to allow operation on C5000™ DSP and C6000™ DSP starter kits (DSK) when used with the 5-6K interface board (*SLAU104*) and the HPA449 Development Board, featuring the MSP430F449 microcontroller. For additional information on using the HPA449 development board, please visit Soft Baugh, Inc. at www.SoftBaugh.com . The EVM can also be operated with simple laboratory equipment, such as a pattern and/or signal generator.

2.1 Parallel Control Connector J4

Five address lines (DC_A0:DC_A4) are available to the EVM through the parallel control connector J4. The EVM uses an SN74LVC138 to address decode the ADS8342's chip select signal. Jumper W11 determines which EVM address the data converter responds to. DC_A0 and DC_A1 provide the ability to select one of four possible address spaces. The actual address space is determined by the connected DSP. Please refer to the DSP Interface section corresponding to your particular processor for details.

The ADS8342's CONV and RD signals connect to the host processors write enable (DC_WE) and read enable (DC_RD) signals. Channel selection via the ADS8342's A1 and A0 pins are controlled by address lines DC_A2 and DC_A3. This allows the host processor to *write* a conversion start command to a specific channel.

Additional signals on the parallel control connector include TOUT and DC_INT. The TOUT signal allows a conversion clock derived by the host processor to be fed to the ADS8342 via jumper W8. The BUSY signal from the ADS8342 is fed via DC_INT to the host processor to act as an interrupt source, indicating that valid data is ready to be transferred.

Table 1. Parallel Control Connections

EVM Connector Pin No.	Connects to ADC Signal Pin	Signal Description / Host Processor Function
J4.1	none	DC_CSa – Enables the EVM's data output buffer, U3
J4.3	CONV	DC_/WE – Host writes to ADS8342 to signal a start of conversion. Used in conjunction with J4.7 – J4.13
J4.5	RD	DC_/RD – Host reads from the ADC
J4.7	CS by U7	EVM_A0 – Used in conjunction with EVM_A1 and U7 to develop the chip select to the ADS8342
J4.9	CS by U7	EVM_A1 – Used in conjunction with EVM_A0 and U7 to develop the chip select to the ADS8342
J4.11	A1	EVM_A2 – Used for input MUX control of the ADS8342
J4.13	A0	EVM_A3 – Used for input MUX control of the ADS8342
J4.15	none	EVM_A4 – Unused for this design
J4.17	TOUT	TOUT – Used in conjunction with W8 to provide the ADS8342 with a processor controlled conversion clock
J4.19	BUSY	DC_INT – Used as an interrupt source to the host processor to indicate valid data is ready for transfer from the ADC's data buffer

2.2 Parallel Data Connector J3

The lower 16 data lines from the host processor are connected directly to the ADS8342 EVM aligned LSB to LSB. Table 1 shows the connections incorporated on the evaluation module for the ADS8342 and the parallel data connector, J3.

Table 2. Parallel Data Connections

EVM Connector / Pin No.	ADC Pin No.	Signal Description
J3.1	16	DB_D0 – LSB from the ADS8342
J3.3	17	DB_D1
J3.5	18	DB_D2
J3.7	19	DB_D3
J3.9	20	DB_D4
J3.11	21	DB_D5
J3.13	22	DB_D6
J3.15	23	DB_D7
J3.17	26	DB_D8
J3.19	27	DB_D9
J3.21	28	DB_D10
J3.23	29	DB_D11
J3.25	30	DB_D12
J3.27	31	DB_D13
J3.29	32	DB_D14
J3.31	33	DB_D15 – MSB from the ADS8342
J3.2 – J3.32 even	n/a	Digital ground connections

3 Setting Up the DSP

The following sections provide an overview of the hardware configurations used for each of the DSPs mentioned in this application note.

3.1 TMS320C6711DSK

The following section provides details on the setup of the TMS320C6711 DSK and the 5-6K interface board for use with the ADS8342 EVM.

3.1.1 Set Up the Conversion Clock and EXT_4

The DSP's internal timer, TOUT0, can be used as the conversion clock source for the ADS8342EVM. For the purpose of this application note, the clock is set for 50/50 duty cycle and a division multiple of 16. This provides approximately a 4.5 MHz conversion clock to the converter. An external conversion clock can also be applied through SMA connector (EXT_CLK) by moving jumper W8 from pins 2-3 to pins 1-2. The maximum clock conversion clock rate is 5 MHz. The timer is configured in the chip support library (CSL) portion of the DSP/BIOS configuration file (ADS8342_6711.CDB).

The BUSY signal from the ADS8342 is sent to the EXT_INT4 pin on the TMS320C6711DSK. The interrupt is defined in the *Scheduling/HWI* section of the ADS8342_6711.CDB file. The interrupt is configured to operate on a *high-to-lo*w transition, which actives the EXT4_ISR subroutine in the C6711 code example provided.

3.1.2 Chip Select (CS), Read (RD) and Convert Start (CONV)

Chip select to the ADS8342 is an active-low input signal. When CS is high, the parallel data pins are in a high-impedance state. When CS is low, the parallel data lines reflect the current state of the output buffers. In order to properly read data from the parallel data bus of the ADS8342, the device must be *chip selected*. EVM_A0 and EVM_A1 determine which address activates the CS signal to the ADS8342.

The ADS8342 EVM address lines EVM_A0..EVM_A4 are defined by jumper settings on the 5-6K interface board via W5. When W5 is open, EVM_A0..EVM_A4 correspond to upper address lines DC_A14 to DC_A17. Closing W5 connects the EVM address lines with the lower C6711 address lines DC_A2..DC_A5.

Table 3. ADS8342EVM Address Definitions for TMS320C6711DSK™

Lower Address	Function – Operation	Upper Address
0xA0000000	RD or WR - ADC /CS Address “00”	0xA0000000
0xA0000004	RD or WR - ADC /CS Address “01”	0xA0004000
0xA0000008	RD or WR - ADC /CS Address “10”	0xA0008000
0xA000000C	RD or WR - ADC /CS Address “11”	0xA000C000
0xA000000x	WR – Select CH0 for next conversion	0xA000x000
0xA000001x	WR – Select CH1 for next conversion	0xA001x000
0xA000002x	WR – Select CH2 for next conversion	0xA002x000
0xA000003x	WR – Select CH3 for next conversion	0xA003x000

The ADS8342EVM uses the DSK’s DC_CSa signal as a master chip select for the board. Read (RD) and write (CONV) are also active low signals. When CS is low, the output buffers of the ADS8342 are updated on the falling edge of the RD signal. Data is read into the C6711 on the following rising edge of RD.

3.2 TMS320C5416DSK

The following section provides details on the setup of the TMS320C5416 DSK and the 5-6K interface board for use with the ADS8342EVM.

3.2.1 Set Up the Conversion Clock and EXT_0

The timers of the C5000™ DSP platform are not as flexible as those of the C6000™ DSP platform. For the purpose of this application note, the McBSP CLKXa signal is used to drive the conversion clock of the ADS8342. The McBSPa clock is configured in the chip support library (CSL) portion of the DSP/BIOS configuration file (ADS8342_5416.CDB). The clock source to the ADS8342 EVM is controlled by jumper J14 on the 5-6K interface board.

The BUSY signal from the ADS8342 is sent to the EXT_INT0 pin on the TMS320C5416DSK. The interrupt is defined in the *Scheduling/HWI* section of the ADS8342_5416.CDB file. The interrupt is configured to operate on a *high-to-lo*w transition, which actives the EXT0_ISR subroutine in the 5416 code example.

3.2.2 Chip Select (CS), Read (RD) and Convert Start (CONV)

As with the C6711, the ADS8342 EVM address lines EVM_A0..EVM_A4 are defined by jumper settings on the 5-6K Interface Board via W5. When W5 is open, EVM_A0..EVM_A4 correspond to upper address lines DC_A12 to DC_A15. Closing W5 connects the EVM address lines with the lower C5416 address lines DC_A0..DC_A3. For the TMS320C5416 DSK, the lower address space is used by the CPLD, so only the upper address lines were used in the software example.

Table 4. ADS8342EVM Address Definitions for TMS320C5416DSK

Function - Operation	Upper Address
RD or WR - ADC /CS Address “00”	0x8000
RD or WR - ADC /CS Address “01”	0x9000
RD or WR - ADC /CS Address “10”	0xA000
RD or WR - ADC /CS Address “11”	0xC000
WR – Select CH0 for next conversion	CS address + 0x0000
WR – Select CH1 for next conversion	CS address + 0x1000
WR – Select CH2 for next conversion	CS address + 0x2000
WR – Select CH3 for next conversion	CS address + 0x3000

The output buffer is activated by the RD signal in combination with a valid CS signal by moving jumper W9 on the ADS8342EVM from position 1-2 to position 2-3.

4 ADC Initialization and Operation

The ADS8342 has no internal registers and requires no specific initialization setups. The conversion process begins when the device is chip selected with an appropriate conversion start command. With the TMS320™ DSP family, the write strobe is the easiest way to accomplish this task.

4.1 CONV, A0 and A1

Signal pins A0 and A1 control the channel to be converted. The first rising clock edge under a valid CONV signal begins the conversion process. CONV must be issued with a valid chip select signal. The entire conversion/acquisition process takes approximately 20 conversion clock cycles for a throughput rate of 250 KSPS per channel (at 5 MHz max CLK rate). The following truth table shows the channel selection criteria:

A1	A0	Converted Channel
0	0	Convert channel 0
0	1	Convert channel 1
1	0	Convert channel 2
1	1	Convert channel 3

4.2 BUSY

The BUSY signal is an active high output which indicates the conversion process has begun. BUSY is held high through the entire conversion/acquisition process. BUSY can be used to interrupt the host processor in order to initiate a read cycle. The following figure shows the signal flow for a complete conversion / read cycle.

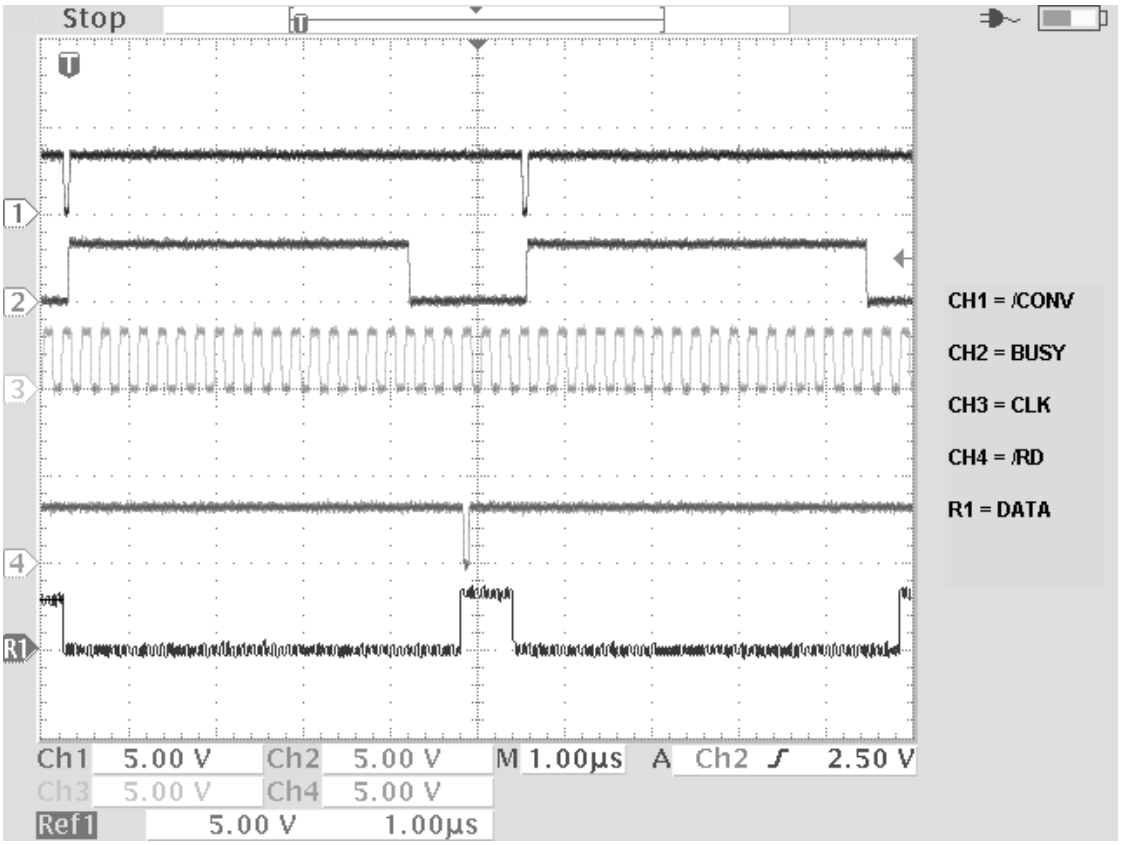

Figure 2. ADS8342 Waveforms

4.3 BYTE

BYTE is an asynchronous signal that allows two consecutive reads to provide the host processor with 8-bit data. When BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BYTE is 1, bits 15 through 8 appear on DB7-DB0. Microcontrollers such as the MSP430 can take advantage of this feature, reducing the number of PORT pins required in the interface.

5 Code Examples

An archive of projects, complete with source and header files associated with this application note is available for download from the Texas Instruments web site. Please enter the document number of this application note (*SLAA176*) into the search windows found at www.ti.com. Click on the link for the abstract to this document and download the associated code files.

The archive is organized into two directories: C6711 and C5416. The complete Code Composer Studio Project files are located in the directories. Simply extract the directory (s) of your choice and open the project file from the Project Manager of Code Composer Studio™.

These files were created with CCS v2.20. Some manipulation of the .CDB file may be required when used with earlier versions of Code Composer.

References

1. *ADS8342, 4-Channel, Parallel Output ADC,* Data Sheet, Texas Instruments Literature Number SBAS277
2. *TMS320C54x DSP CPU Reference Guide,* Texas Instruments Literature Number SPRU131
3. *TMS320C6000 Peripherals Reference Guide,* Texas Instruments Literature Number SPRU190

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