Application Report
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System Design Considerations for True Digital Audio Power Amplifiers

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ABSTRACT

This report describes the conversion of pulse-code-modulated (PCM) to pulse-width-modulated (PWM) signals using Texas Instruments TDAA modulation devices (TAS50xx) and signal amplification using Texas Instruments family of H-bridge output stages (TAS51xx). It includes a detailed discussion of power supply voltage requirements, output circuit filters, and thermal dissipation. An example stereo application shows how to select various components and demonstrates TDAA measurements and what to look for in the results.

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1 Introduction

A true digital audio amplifier (TDAA) chip set consists of a TAS50xx PCM-PWM modulator and a number of TAS51xx PWM amplifiers as shown in Figure 1. At the center of this patented technology is the conversion of pulse-code modulated (PCM) to pulse-width modulated (PWM) signals. The audio signal is maintained in the digital domain right until the last filter before the speaker connection. No analog signal amplification is used, and the PWM signal powers the speakers directly through a passive low-pass filter. This allows the full digital signal chain to pass the high quality audio signal directly to the speaker, without distortion from analog amplification.

The TDAA amplifier can also be viewed as a power DAC with a simple passive low-pass filter.

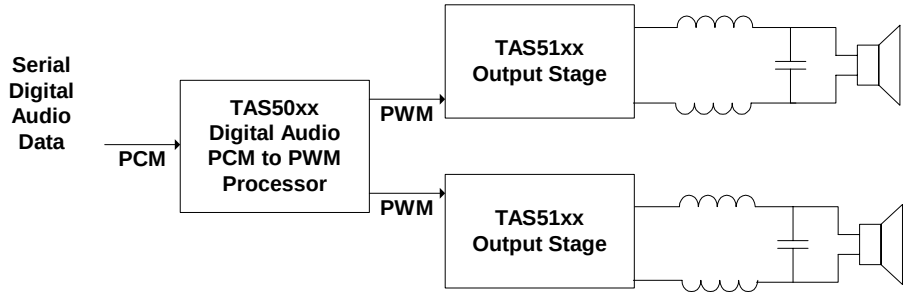


Figure 1. System Block Diagram, Stereo Configuration

1.1 Conversion of PCM to PWM Using TDAA Devices

A sine wave is shown in terms of a pulse-code-modulated signal in the upper panel of Figure 2. In a PCM signal, each discrete sample has an assigned integer amplitude. The corresponding pulse-width-modulated signal at the same sampling rate (frequency) is shown in the lower panel. The magnitude of each PWM sample is described in terms of the pulse *width*, as opposed to the pulse *height* in a PCM signal. The pulse width vs pulse height distinction is shown in Figure 3. The function of the TAS50xx modulator is to perform the PCM-to-PWM signal conversion.

The digital audio (24-bit PCM) signal is fed to the modulator device. Internally, there is a digital interpolation filter where the audio data is up-sampled 2, 4, or 8 times (depending on the sampling rate) to typically 352.8 kHz or 384 kHz, which are the TDAA internal sampling rates. The Equibit modulator then translates the up-sampled signal to a PWM signal having the same switching frequency. The translation from PCM to PWM is nonlinear and the TAS50xx modulator employs sophisticated patented [1] correction algorithms to improve overall system performance.

The PWM signals for each channel are then fed to a TAS51xx power output stage, where the PWM signals are level shifted and fed to two sets of N-channel DMOS power transistors connected in an H-bridge. Finally, the PWM output signal from each TAS51xx is fed to its respective speaker via a passive low-pass filter, typically of second order.

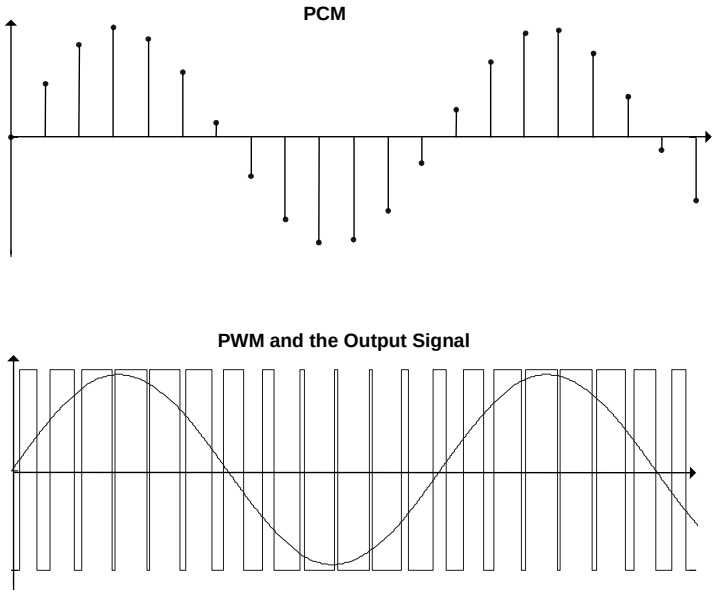


Figure 2. TDAA, PCM, and PWM Signals

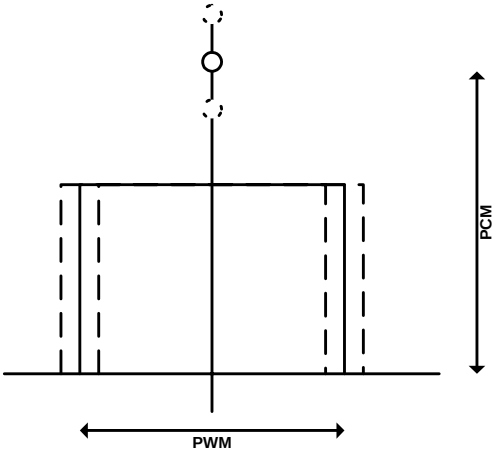


Figure 3. PCM and PWM Modulation

1.2 TDAA Measurements

To perform correct measurements on a TDAA, it is important to understand the characteristics of this type of device. An overview of the technology, its functionality, efficiency and output spectrum, as well as a detailed discussion of making measurements on TDAAs can be found in *Digital Audio Measurements*, Texas Instruments literature number SLAA114 [2].

2 Output H-Bridge of the TAS51xx

2.1 Bootstrap Gate Drive

The TAS51xx includes two dedicated bootstrapped power supplies. Typically, a bootstrap capacitor of 33 nF is connected between the individual bootstrap pin and the associated output. The bootstrapped power supply minimizes the number of high-voltage power-supply levels externally supplied to the system, while providing a low-noise supply level for driving the high-side N-channel DMOS transistors.

2.2 Gate Driver Voltage Regulator

The TAS51xx provides two on-chip low-dropout voltage regulators (LDO) to minimize the number of external power supplies needed for the system. These voltage regulators are for the internal circuits only and can not be used for external circuitry. The LDO output voltage must be decoupled by a 100-nF capacitor to ground (PVSS).

3 Power Supply and Decoupling

TDAA audio amplifier technology is a direct PCM-to-PWM converter without feedback; this requires good decoupling and a good power supply. The power supply voltage needs to be regulated because the H-bridge is switching the supply level directly to the outputs via the output reconstruction filter. The power supply in a TDAA amplifier can be regarded as a voltage reference in a DAC.

Changes in the power supply act as a volume change and, in fact, by having a power supply to the output stage that is varied logarithmic, this can be used as a volume control. Normally, digital volume control is easier to implement. Texas Instruments digital audio processors, such as the TAS3001 or the TAS3002, can implement volume, bass, and treble control, and can also do parametric equalization completely in the digital domain.

3.1.1 Requirements for Power Supply

The voltage supply required can be calculated using equation 1.

$$V_{SS} = \frac{\left[Z_{(load)} + 2(R_{(DMOSon)} + R_{(ind)}\right]\sqrt{2P_{(max)} / Z_{(load)}}}{M} \quad (1)$$

where $P_{(max)}$ is the maximum output power, $Z_{(load)}$ is the load impedance, $R_{(DMOSon)}$ is the DMOS transistor on-state resistance, $R_{(ind)}$ is the output inductor series resistance, and M is the maximum PWM modulation. For the TDAA chip set, M = 0.9 coming from the PCM to the PWM modulator. To dissipate 25 W with 4 Ω, a power supply voltage of 18.9 V is needed, and 19 V is satisfactory.

The TDAA output stages have a power efficiency above 85%, so the power supply must feed the TDAA amplifier with 25% more power than the maximum average output power. For 25 W of output power per channel, the system's (two speaker) average power supply requirement is:

$$P_{(avg)} = 2P_O / \eta = 58.9 \text{ W} \quad (2)$$

This is the average power from the supply. When delivering power to the load sinusoidally, the peak power, P_{TM}, is actually twice as high as the average (RMS) power:

$$P_{TM} = 2P_{(avg)} = 125 \text{ W} \quad (3)$$

Figure 4 shows the instantaneous power-supply current draw needed to drive two 25-W 4-Ω speakers. The peak current draw from a 19-V supply is a substantial 6.6 A.

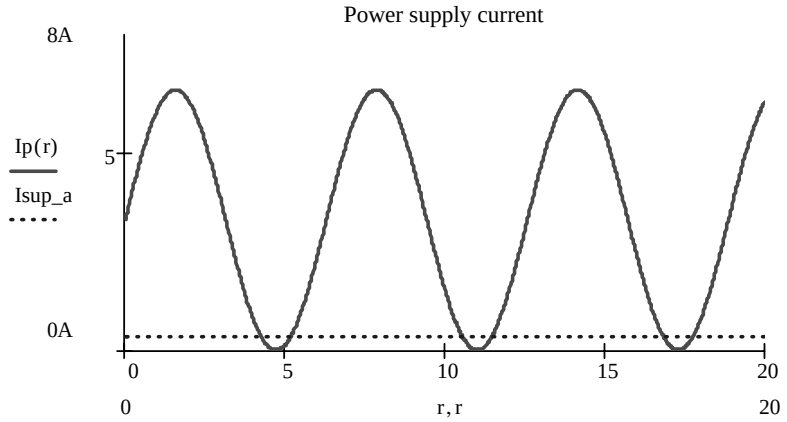


Figure 4. Instantaneous and Average Working Power Supply Current

Because of the dynamic nature of music, when delivering music to a speaker there is a dramatic reduction in the average power consumption—a peak to average power range of more than 20 dB is normal—so a power supply that can deliver the maximum output power continuously is unnecessary. In fact, a good compromise is 1/8 of full power. The dashed horizontal line in Figure 4 is the current corresponding to 1/8 of the maximum power output level (6.25-W output power), but the PSU needs to be capable of delivering the peak power required.

A typical music CD requires 12 dB to 15 dB of dynamic headroom above the average power output to pass the loudest portions without distortion. This is a good fit with the compromise of a continuously rated power supply having 1/8 power output. According to CIRSP22, 1/8 full power is the level at which testing is to be carried out during EMI qualification.

3.1.2 Selection of Capacitors

The decoupling capacitors need to withstand the ripple current from the switching stage, as well as supply the audio current. The ripple current is calculated from the switching frequency (352.8 kHz), the supply voltage (19 V), and the output inductance value (10 μH):

$$I_{(RMS)} = \frac{V_{SS}}{2 \times 2 \times 2\sqrt{3}\, L\, f_{(S)}} = 0.387 \text{ A}$$

This is the idle current in the bulk power supply capacitor for each H-bridge. For a 25-W output load and a 19-V supply, the audio current load is:

$$I_{(audio)} = P_O / V_{SS} = 1.316 \text{ A}$$

The total current draw is then:

$$I_{(total)} = \frac{I_{(audio)}}{8} + I_{(rms)} = \frac{1.316}{8} + 0.387 = 0.533 \text{ A}$$

The capacitor need not be rated for continuous peak-power output, so a ripple current capability of 0.5 A should be sufficient.

There is a direct relationship between the amplifier distortion and the output impedance of the power supply, which includes the decoupling capacitors. At low frequencies the regulated power supply has low-output impedance; however, at high frequencies the decoupling capacitors act as a low-impedance source. Therefore, the series resistance of the chosen electrolytic capacitors needs to be kept low. The required capacitor series resistance from the output THD is:

$$R = \frac{4(THD)R_{(load)}}{M^2}$$

The THD is not the total THD but is the figure coming from output resistance of the power supply, hence, the bypass capacitor equivalent series resistance, ESR. For M = 0.9; THD = 0.2%; and $R_{(load)}$ = 4 Ω, the capacitor series resistance is:

$$R = \frac{4 \times 0.002 \times 4}{(0.9)^2} = 0.04\ \Omega$$

Suggestions for capacitor types are offered in the *Component Selection* section of this report.

4 Reconstruction Output Filter

The TDAA amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either off or fully on, which reduces the DMOS transistor on-state resistance, $R_{(DMOSon)}$, and the power dissipated in the device, thereby increasing efficiency. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. For this application EMI is considered important; therefore, the selected filter is the full output type shown in Figure 5.

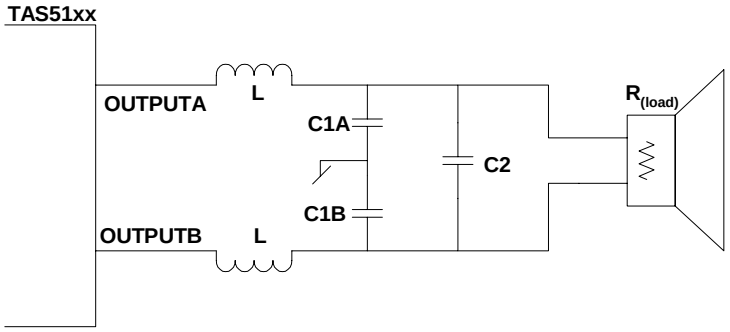


Figure 5. TDAA Output Circuit and Filter

The main purpose of the output filter is to attenuate the high-frequency switching component of the TDAA amplifier while preserving the signals in the audio band.

This low-pass filter is specified by its cut-off frequency (-3 dB), its gain and ripple in the pass band, and its attenuation in the stop band. The order of the filter determines how many poles exist at the same frequency, with each increase in order increasing the attenuation above the cutoff frequency by –20 dB per decade. The switching frequency of the amplifier can influence the selection of the filter's order—the higher the switching frequency; the lower the order required to achieve a given attenuation within a specified pass band. This suggests using the highest switching frequency possible. The tradeoff is that increasing the switching frequency increases both the switching losses and the EMI, and it decreases the efficiency of the amplifier.

A second-order low-pass filter reduces the switching frequency by –40 dB per decade to one percent of its prefiltered value. A 5-V signal at 352.8 kHz is reduced by –40 dB over one decade to 50 mV. If increased attenuation is desired, there are two alternatives that remain: implement a higher order filter which increases the number of components and the cost, or increase the switching frequency, which reduces the overall efficiency and increases EMI.

4.1.1 Filter Design

The output filter is a simple, second-order LC-type filter designed using a Butterworth approximation. This type of filter is desirable for the relatively-flat pass-band response it provides and for the small number of parts it requires. The transfer function for a second-order Butterworth filter is:

$$H(s) = \frac{1}{s^2 + \sqrt{2}\,s + 1} \tag{3}$$

The first step in designing the filter is to construct the circuit and derive the transfer function, starting first with a half-circuit model and moving later to the full-bridge circuit. The half-circuit model of the Butterworth low-pass filter output is shown in Figure 6, with only one-half of the desired dc load resistance, $R_{(load)}$, of the speaker shown. The input signal, $V_{(in)}$, is the 352.8-kHz square-wave output of the TDAA amplifier, while the output, V_O, is the voltage developed across the speaker.

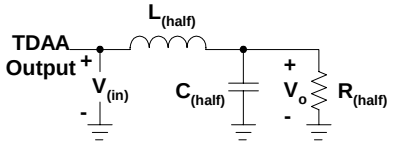


Figure 6. Butterworth Low-Pass Filter Half-Circuit Model

The transfer function for this half circuit is:

$$H(s) = \frac{\dfrac{1}{L_{(half)}C_{(half)}}}{s^2 + \dfrac{1}{R_{(half)}C_{(half)}}s + \dfrac{1}{L_{(half)}C_{(half)}}} \tag{4}$$

The component values are:

$$C_{(half)} = \frac{1}{2\sqrt{2}\pi f_{co} R_{(half)}} \tag{5}$$

And

$$L_{(half)} = \frac{R_{(half)}}{\sqrt{2}\pi f_{co}} \tag{6}$$

The two half-circuit models are now combined to yield the actual bridge-tied load (BTL) circuit shown in Figure 7 and the capacitors and resistors are combined to provide the final BTL equations.

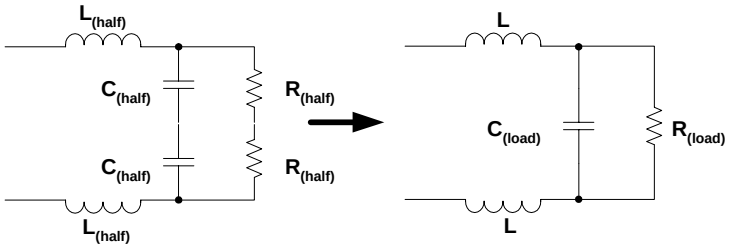


Figure 7. Combination of Two Half-Circuit Models

$$R_{(load)} = 2R_{(half)} \tag{7}$$

$$C_{(load0} = \frac{1}{2\sqrt{2}\pi R_{(load)} f_{co}} \tag{8}$$

$$L = L_{(half)} = \frac{\sqrt{2}\, R_{(load)}}{4\pi f_{co}} \tag{9}$$

The inductance value is the same for the half- and full-bridge circuits because there are two inductances in the BTL circuit. Based on these BTL component values, the –3-dB cutoff frequency for the LC filter is:

$$f_{co} = \frac{1}{2\pi\sqrt{2\, L\, C_{(load)}}} \tag{10}$$

where the $\sqrt{2}$ in the denominator is the result of transposing the inductance and capacitance values from the half circuit to the full BTL-circuit model.

The capacitors labeled C1A and C1B in Figure 5 serve as high-frequency bypass capacitors acting as a common-mode filter and are empirically chosen to be approximately 10% of 2 x $C_{(load)}$.

The choice of filter components and cutoff frequency is a highly individual task because the load impedance is not constant—it varies from speaker to speaker.

4.1.2 Design Example

A TDAA audio system is to be designed with a pass band of 20 Hz to 20 kHz and a switching frequency of 352.8 kHz. The pass-band attenuation at the switching frequency is to be 40 dB, and the corner frequency of the low-pass filter is to be set to avoid attenuation of audio signals by more than 1 dB across the audio spectrum. Each speaker's dc-resistance is 4 Ω, and a second-order LC filter is to be used. What inductor and capacitor values are required?

The capacitances and inductances are calculated using the BTL equations 11 and 12.

$$C_{(load)} = \frac{1}{2\sqrt{2}\,\pi R_{(load)} f_{co}} = \frac{1}{2\sqrt{2}\times 4\times 35\,800} = 786 \text{ nF} \tag{11}$$

$$L = L_{(half)} = \frac{\sqrt{2}\,R_{(load)}}{4\pi f_{co}} = \frac{\sqrt{2}\times 4}{4\pi\times 35\,800} = 12.6\,\mu\text{H} \tag{12}$$

Equation 10 provides a check on the calculation, when it is applied, these values are found to be correct. Reviewing available component values shows options for L of 10 µH and 15 µH, and the closest values for $C_{(load)}$ are 680 nF and 1 µF. Selecting values of 1 µF and 10 µH for $C_{(load)}$ and L, respectively, pushes the cut-off frequency out to 35.6 kHz.

Except for the high-frequency bypass capacitors labeled C1A and C1B in Figure 5, the filter is now complete. These capacitors should be approximately 10% of 2 x $C_{(load)}$, or 200 nF. The nearest standard value is 220 nF, which brings the cutoff frequency to 33.8 kHz.

4.1.3 Component Selection

The output inductors are one of the key elements in determining the performance of the TDAA audio power amplifier system. The most important specifications for the inductor are its resistance and its dc- and peak-current ratings. The resistance directly impacts the efficiency by adding to the total load resistance seen by the power supply. The efficiency is approximately:

$$\eta = \frac{P_{(out)}}{P_{(in)}} \approx \frac{I^2 R_{(load)}}{I^2[2(R_{(DMOSon)} + R_{(ind)}) + R_{(load)}]} = \frac{1}{1 + 2\,\dfrac{R_{(DMOSon)} + R_{(ind)}}{R_{(load)}}} \tag{13}$$

As before, $R_{(load)}$ is the dc-resistance of the speakers, $R_{(DMOSon)}$ is the on resistance of the DMOS power transistors, and $R_{(ind)}$ is the dc-resistance of the inductors.

The inductor current ratings must be high enough to avoid magnetic saturation, which causes an increase in audio signal distortion or, if completely saturated, causes the inductor to appear as a short rather than an open circuit to the PWM output. Potentially, complete saturation could damage the device or speakers as a result of the high current surge that can occur during turn on, or from the increased quiescent current during normal operation. It is best to choose an inductor that has a much higher current rating—the penalty is increased inductor size and cost.

The filter capacitor, C2, must be able to handle the output RMS voltage at the maximum output frequency. The filter capacitors C1A and C1B must be rated to handle the sum of the dc and ac voltages, namely $V_{SS} / 2 + \sqrt{P_{(max)} R_{(load)} / 2}$, where V_{SS} is the power supply input voltage, $P_{(max)}$ is the maximum RMS power output for the amplifier, and $R_{(load)}$ is the dc resistance of the speaker. This is the minimum supply voltage needed, and allowances must be made for temperature, applied voltage, and transient voltage spikes. As a rule of thumb, the voltage rating should be twice what is calculated.

The filter capacitors need to be able to withstand the full audio signal at 20 kHz, e.g., for a 25-W amplifier feeding a 4-Ω load; the required voltage rating is 10 V RMS at 20 kHz.

Metal-film type is the best choice for the main filter capacitor C2. However, ceramic capacitors with X7R characteristics also may be used for C1A and C1B.

5 Design of Switching Circuits

5.1.1 EMI Control

Controlling EMI can be such a tedious job that it is often regarded as magical. However, with careful PCB layout and control of oscillation on the switching waveforms, EMI control is quite manageable.

All wires and connections (effectively, antennas) going to and from the TDAA must be filtered and decoupled. The main power supply requires a local filter on the PCB board of the TDAA; speaker outputs also require high-frequency filters that must be decoupled with RC circuits. The serial digital audio input data also needs to be filtered and decoupled to earth or a chassis ground.

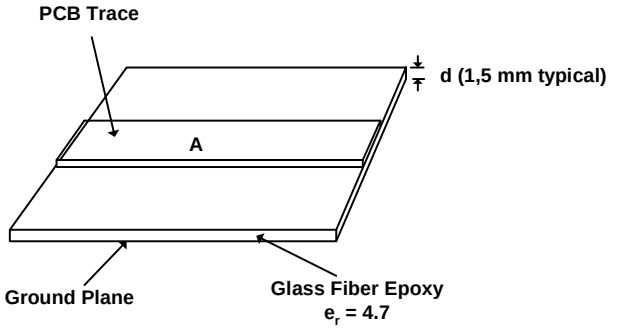
5.1.2 Controlling Stray Inductance and Capacitance

In addition to dc resistances, PCB traces and wires also have parasitic ac components in the forms of inductance and capacitance. This ac impedance interacts with the pulsating currents and voltages in the TDAA circuits and can cause oscillation, which degrades the EMI and audio performance.

Trace Capacitance:

A PCB trace that runs above a ground plane is an example of the parallel plate capacitor (see Figure 8). The total area of the trace, the separation between the trace and the ground plane, and the dielectric constant of the PCB material, determines the amount of capacitance.

A trace on the top layer with a width of 5 mm and a length of 50 mm on a 4-layer PCB with the ground layer as layer 2 is equivalent to a 28-pF capacitance. So if there is a power-supply plane decoupled with a ceramic capacitor, then there are in effect two capacitors with an inductance between them—the result is oscillation. To avoid oscillation, minimize the power plane (not the ground plane), and only use tracks in the power supply.



A = plate area in mm^2
d = plate separation in mm
e_r = dielectric constant relative to air

$$C := \frac{8.85 \cdot 10^{-12} \cdot e_r \cdot A}{d}$$

Figure 8. Trace Capacitance

Trace Inductance:

The equation for the inductance of a trace is:

$$L = 2 \times 10^{-7} \times l \left[\ln \frac{2.1}{w+h} + 0.2235 \frac{w+h}{l} + 0.5 \right]$$

where l is the trace length, w is its width and h is its height (or thickness). Thus, a 100-mm long trace with a width of 0,25 mm and a thickness of 38 μm has an inductance of 141 nH.

Keeping the components close together and having point-to-point routing minimizes the stay inductances.

5.1.3 Damping Oscillations

Adequate damping and control of oscillations are key issues when designing with switching circuits such as a TDAA. In the present design example, the following nodes are dampened with RC circuits.

- Bulk power supply voltage (19-V power supply)
- H-bridge power supply inputs, PVDDA1 and PVDDB1
- Speaker terminals, positive and negative

With an oscillating circuit having a stray inductance, $L_{(s)}$, and a stray capacitance, $C_{(s)}$, the damping RC circuits can be calculated using:

$$R_{(rc)} = \tfrac{1}{2} \sqrt{\frac{L_{(s)}}{C_{(s)}}}\ ; \qquad C_{(rc)} = 3 C_{(s)}$$

For a stray inductance and capacitance of 20 nH and 100 pF, respectively, the calculation shows that a 7-Ω resistor and a 300-pF capacitor are required for the RC circuit.

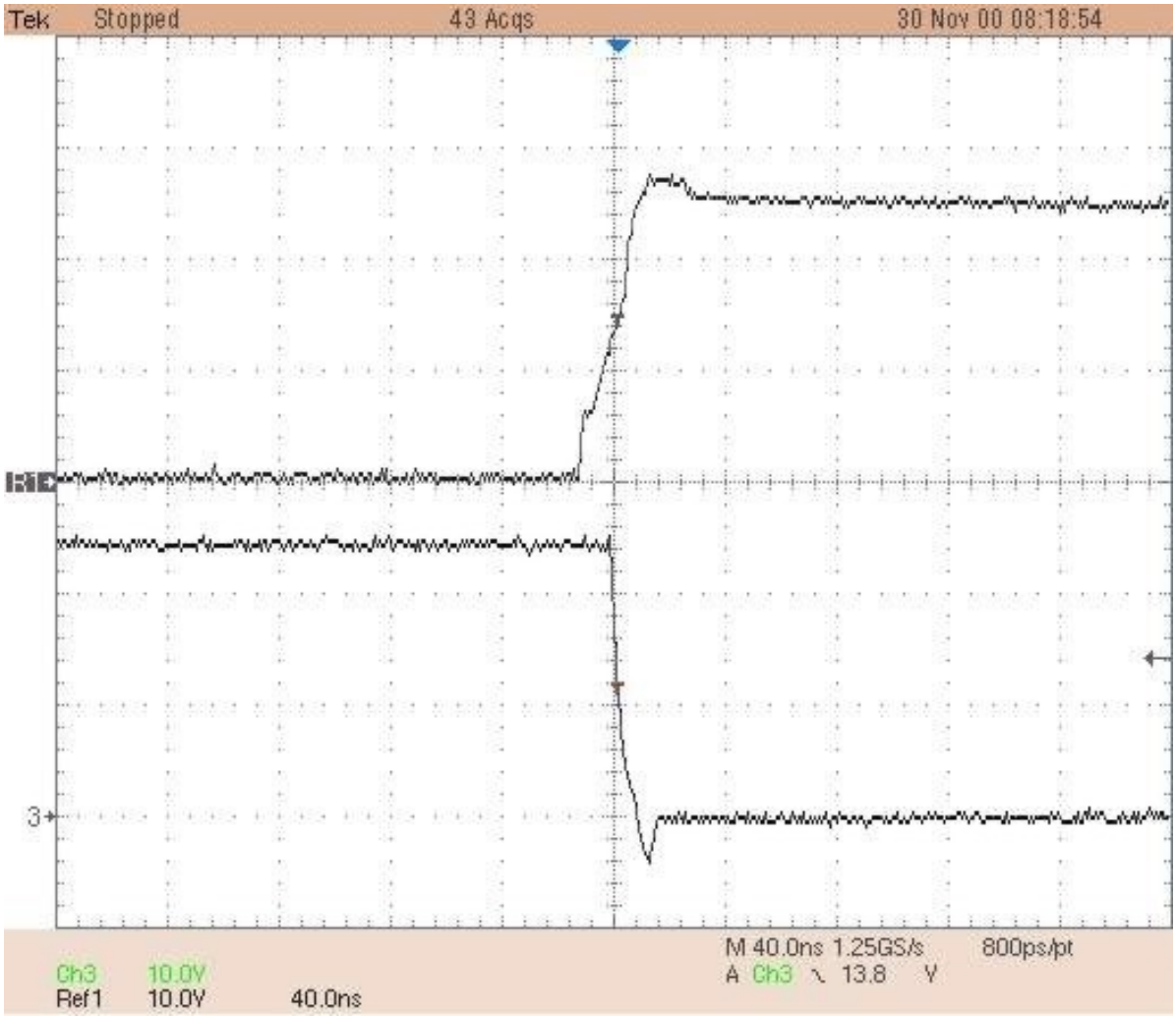


Figure 9. Sample TAS51xx PWM Output Waveform

Figure 9 shows the well-controlled PWM waveform that is obtained when the recommended RC-circuits and PCB layout are used in this application example. The upper trace shows the PWM signal going from low to high, and the lower trace shows the PWM signal going from high to low. The supply voltage was 24 V for this setup. The figure also shows the very fast rise and fall times, with a well-damped waveform. Only half ringing is seen during the transition.

6 Thermal Design of PowerPAD™ PCB Layout

6.1.1 Thermal Design With PowerPAD

The thermally-enhanced DAP package, used in mono H-bridges such as the TAS5100, is based on the 32-pin HTSSOP, but it includes a thermal pad (see Figures 10 and 11) to provide an effective thermal contact between the IC and the PCB.

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Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220 type packages have leads formed as gull wings to make them usable in surface-mount applications. These packages, however, do not have a terminal count high enough to accommodate the TDAA output stage with protection and control. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of the TDAA output stage.

The PowerPAD package (thermally enhanced HTSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages and is designed to optimize the heat transfer to the PCB. Because of the small size and limited mass of a HTSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the TDAA chip. When this pad is soldered or otherwise thermally coupled to an external heat dissipater, high power dissipation in the ultrathin fine-pitch surface-mount package is reliably achieved.

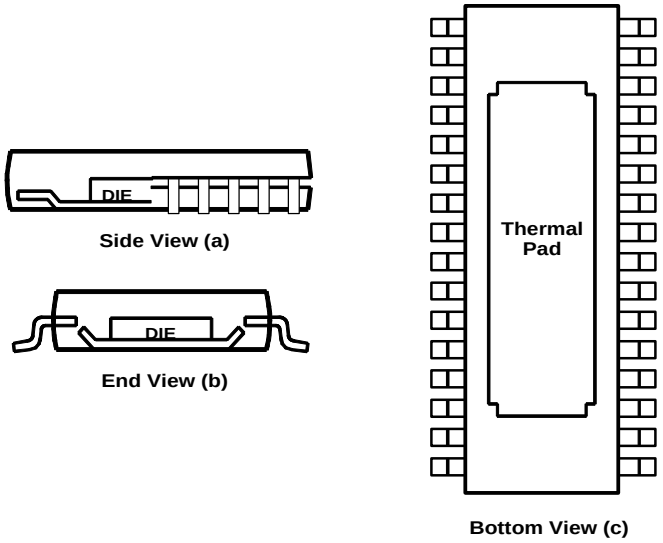


Figure 10. Views of Thermally Enhanced DAP Package for TAS5100

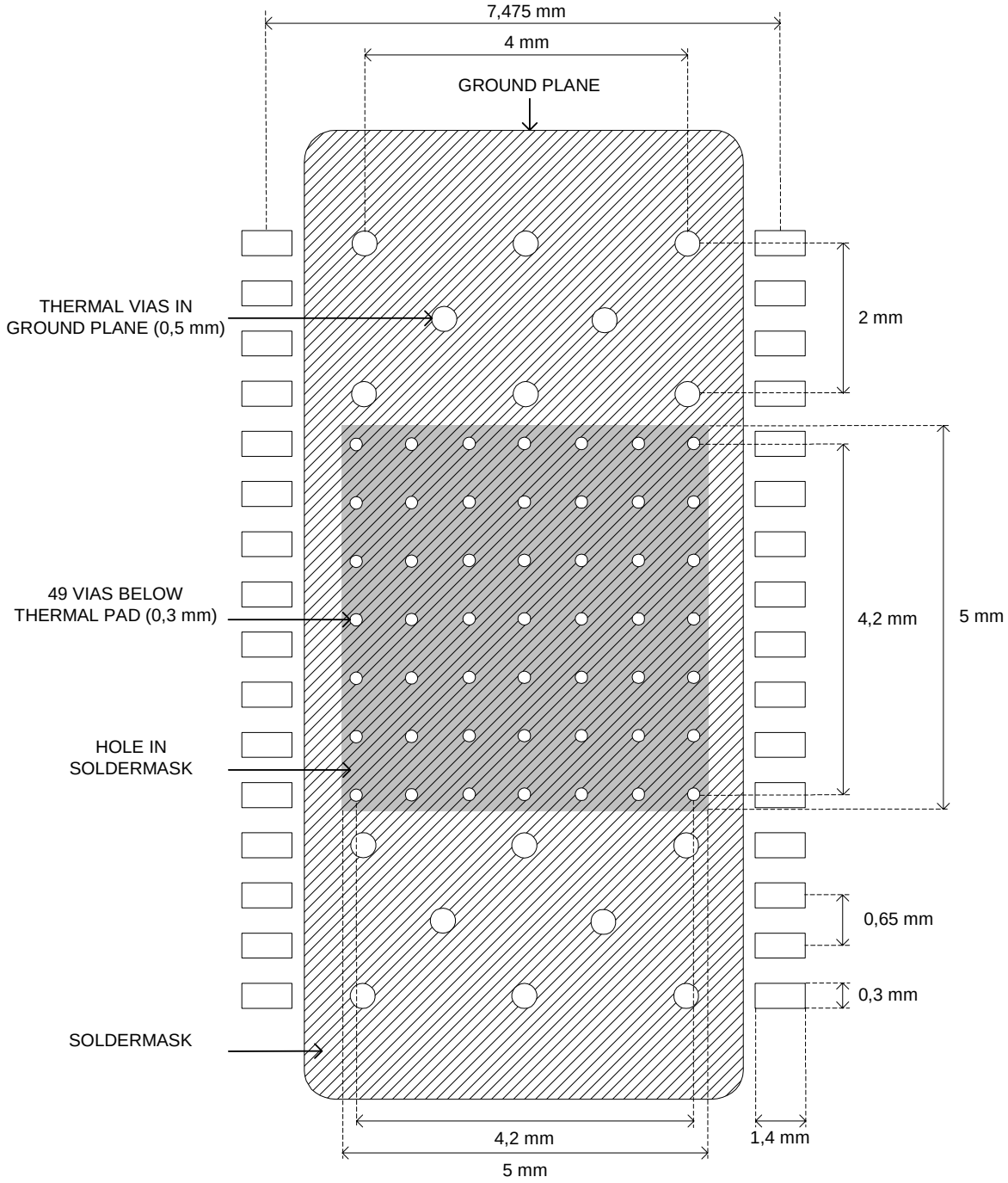


Figure 11. Recommended TAS5100 PCB Land Pattern

For operation at temperatures in excess of ambient (25°C) the DAP package's power capability must be derated according to the data in Table 1.

Table 1. Dissipation Derating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DAP	5.3 W	42.5 mW/°C	3.4 W

It is important to maximize the size of the copper area used as a heat sink for the device. All layers of the PCB can be used to spread the heat into the PCB, e.g., a ground plane also increases the thermal performance. In the application example shown in the following section, the top and bottom layers have been filled with ground-connected copper used as a heat sink—this gives a low-impedance ground plane. For further information on PowerPAD, see the *PowerPAD Thermally Enhanced Package* application report, Texas Instruments literature number SLMA002 [5]. For information on using other H-bridges package styles, consult the individual device data sheet.

6.1.2 Ground Plane

The use of a single ground plane is recommended for this application. In the TDAA amplifier there is no analog signal processing such as there is when using DAC's; therefore, only a digital ground plane is needed.

The ground plane makes it possible to have good decoupling and low inductances in the ground returns for the different signals in the circuits. This is important for the output filter of the PWM output stage. First, in the high power supply feeding the output stage, there are large ripple currents that require low-inductance paths of the ground plane. Secondly, the ground plane gives good return paths for the digital input signals, and for the transmission of the PWM signals between the TAS50xx and the TAS51xx.

For controlling the EMI of this digital amplifier, the use of the ground plane is almost mandatory because the ground plane makes it possible to limit the emissions from the digital master clocks, the PWM output switching and any stray oscillations from the various circuits.

The ground plane also acts as heat sink for the 2-layer H-bridges using the DAP package.

The application example in the *Measured Performance of Application Example* section shows a PCB with a maximum ground area in both the top and bottom layers.

6.1.3 Output Stage and Bulk Power

Allowing for output stage switching requires special care during PCB board layout. The TAS51xx pinning has been laid out to facilitate good routing of the output stage. It is recommended to use point-to-point routing of the bulk power supply, i.e., in connecting to the PVDDA1 and PVDDB1.

The inductance of the track connecting the bulk power capacitor to the H-bridge is a critical factor in managing performance and EMI. Inductance values between 50 nH and 75 nH are ideal, corresponding to track lengths in the region of 55 mm. PVDDA1 and PVDDB1 should have there own inductor, damped by an RC network as described in the *Damping Oscillations* section. Both inductive tracks in the layout should be the same length from the bulk capacitor to the H-bridge, and the routing from the power input connector to each bulk capacitor should be equal distances, with the least possible shared copper.

7 Measured Performance of Application Example

This section describes the measured performance of a stereo TDAA amplifier with 30 W of output power per stage, with each stage supporting a 6-Ω load. The amplifier is powered by a single 23-V supply and has onboard regulators to provide the 5-V and 3.3-V power sources required by the digital circuits. The set up includes the following components: a SPDIF receiver (DIR1703), digital volume control with parametric equalizer (TAS3002), and the TDAA amplifier chip set (a TAS5010 and two TAS5100 devices).

7.1 Performance Measurements

This section discusses the performance measured on the application example using a 23-V power supply and two 6-Ω load impedances. Measurements were made in accordance with the guidelines presented in the *Digital Audio Measurements* applications report, Texas Instruments literature number SLAA114 [1], for class-D amplifiers.

7.1.1 THD+N vs Frequency

The measurements in Figure 12 show that the distortion is nearly independent of the frequency. At a normal listening level of 1 W, the sound quality is very high.

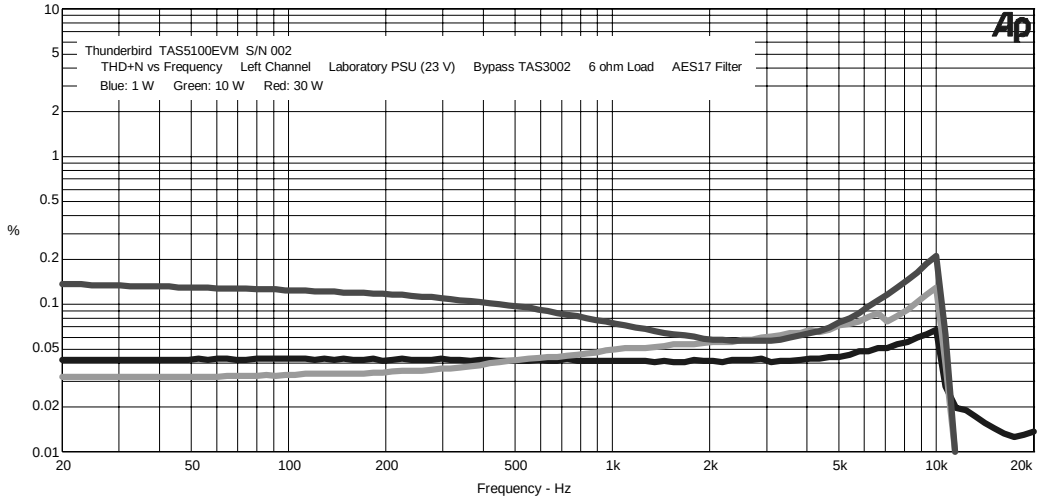


Figure 12. THD+N vs Frequency

7.1.2 THD+N vs Output Power

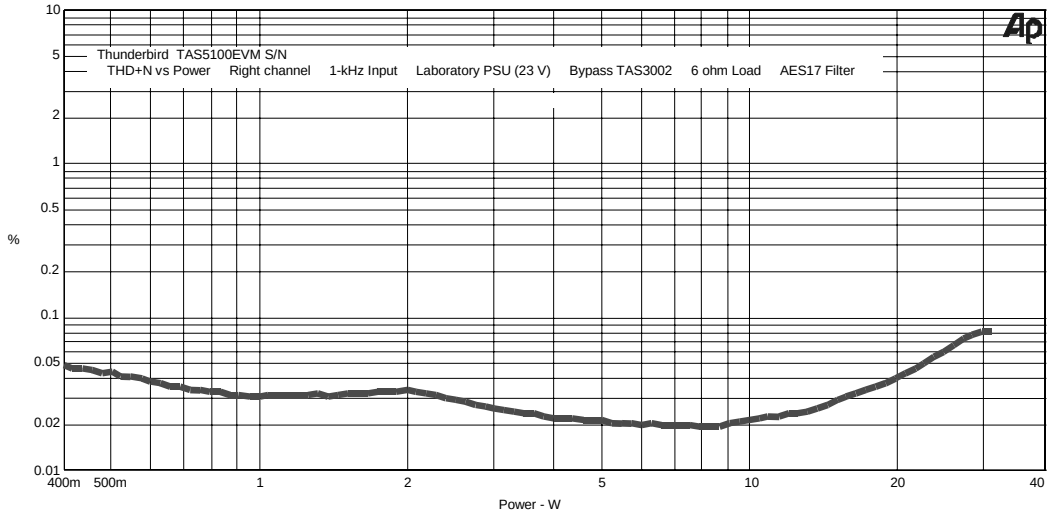


Figure 13. THD+N vs Output Power

THD+N is a sum of all the output errors, including noise, various harmonic distortions and hum from 60-Hz operated equipment. The THD+N measurement shows a very characteristic shape for the TAS5000 and TAS5100 chip set. At the low-output power of 1 W, the THD+N is dominated by noise. Above 10 W, the distortion from the output stage and the output filter dominate the THD+N curve. See the *Digital Audio Measurements* applications report, Texas Instruments literature number SLAA114 [1], for further explanation on the distortion curves.

7.1.3 Noise Floor

Figure 14 shows a 16K FFT with a –60-dB sinusoidal tone. Zero decibels correspond to the maximum output of the amplifier without clipping. The results are a very flat noise floor and low distortion. The A-weighted signal-to-noise ratio for this TDAA example is 93 dB measured at the speaker terminals.

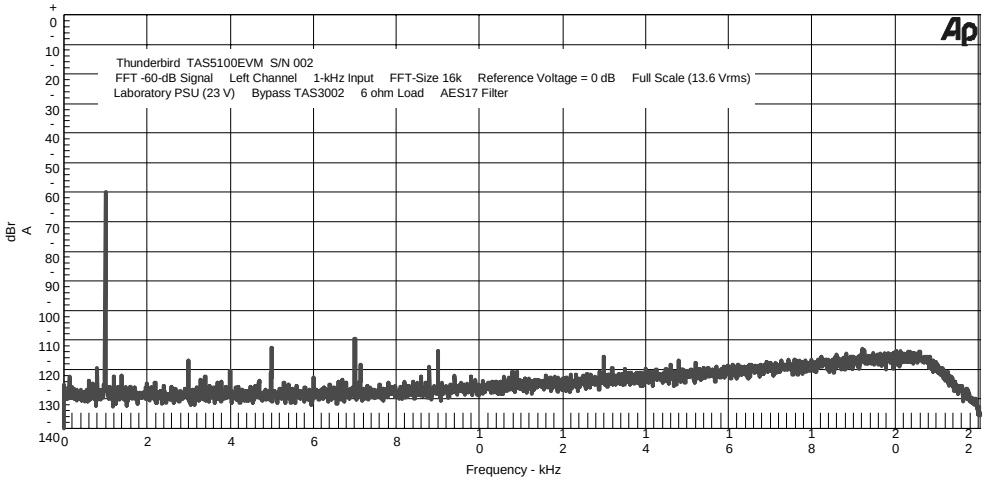


Figure 14. FFT With –60 dB

7.1.4 Frequency Response

The frequency response curve of Figure 15 shows the small rolloff at 20 kHz from the output filter. This rolloff varies with load impedance (see the calculations in the *Reconstruction Output Filter* section).

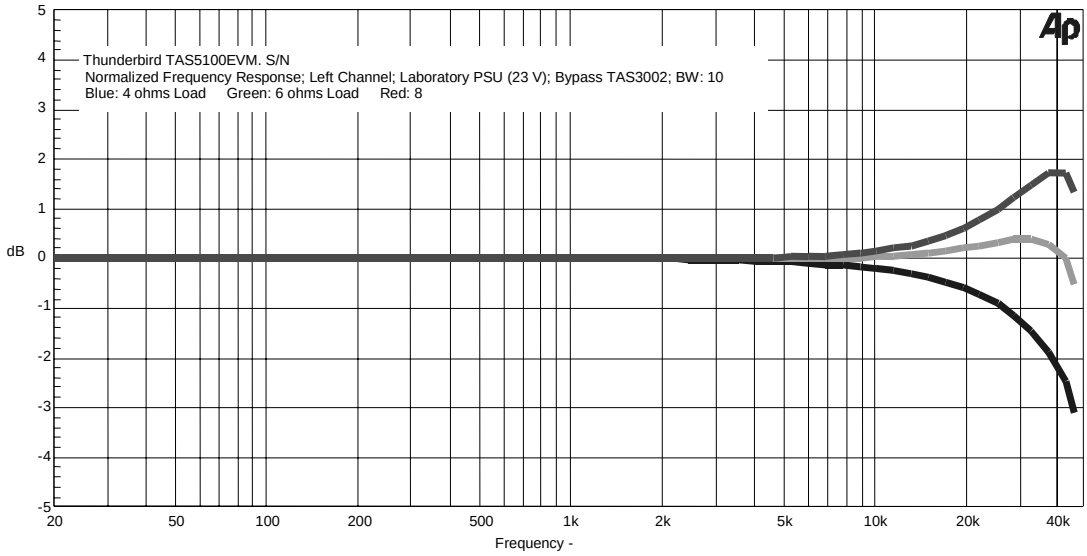


Figure 15. Frequency Response With a 6-Ω Load

7.1.5 Power Efficiency

The ideal muted power consumption is 0.68 W; running the power consumption is 3.3 W. The efficiency curve shown in Figure 16 is for a 6-Ω load; if the amplifier were loaded with 8 Ω, the efficiency would increase.

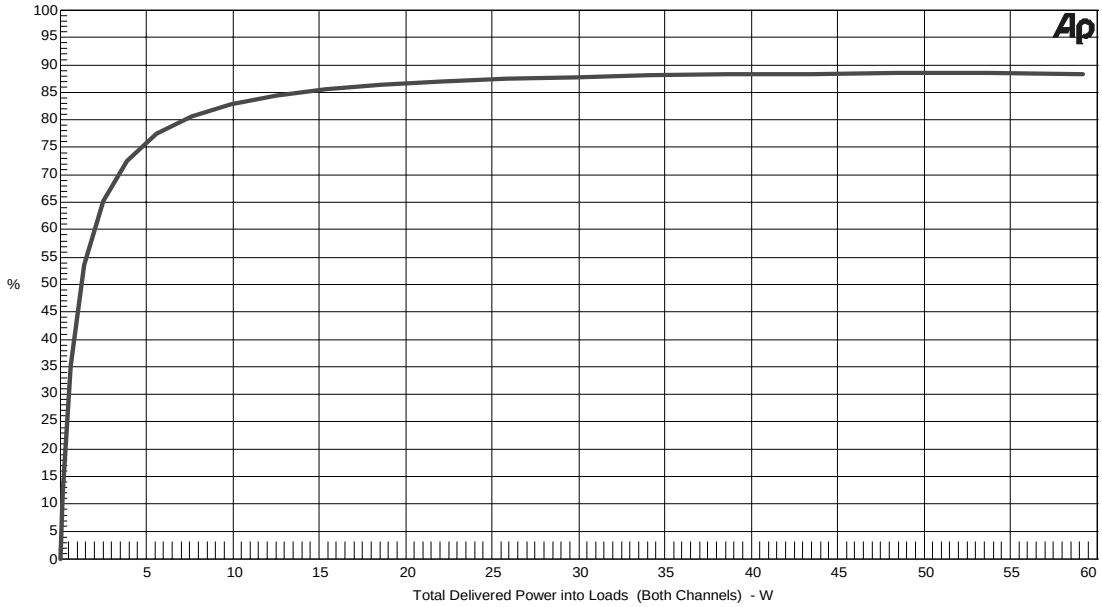


Figure 16. Measured Power Efficiency (η) vs Power

7.1.6 EMI Measurements: Radiated Emission

Radiated emission was measured over the range from 30 MHz to 1 GHz using the test setup and test equipment shown in Tables 2 and 3, respectively.

Table 2. EMI Measurements: Test Setup

ITEM	TEST SETUP DESCRIPTION
DUT	Prelude assembly, no lid on enclosure
Input signal	1-kHz sine wave, source: CD player located outside ferrite room
Load	4-Ω dummy load (each channel)
Output power	Corresponding to1/8 of 30 W on each channel
Speaker cable	Two, 3-meters long

Table 3. EMI Measurements: Test Equipment

ITEM	SETUP
Equipment	EMC test facility for radiated emission measurements. (Ferrite room), 3-m antenna distance.
Detector	Peak / Quasi peak
Limit	According to EN 55022; same as CFR45 part 15 class B (limits shown according to a 3-m antenna position)
Frequency range	30 MHz to 1 GHz

Figure 17 shows a maximum-hold frequency scan covering vertical and horizontal antenna positions and 360° rotation of the DUT. The test result shows a very flat appearance with no distinct frequency components. The solid line in Figure 17 shows the emission limit according to EN55022 (same as CFR47 Part 15 class B). If the dashed line is the 10-dB limit line, if exceeded, would require an open area test site (OATS) validation. For this setup, the spectrum stays below the dotted line at all frequencies—an OATS validation of the measurement is not needed, and the setup passes the EMI test.

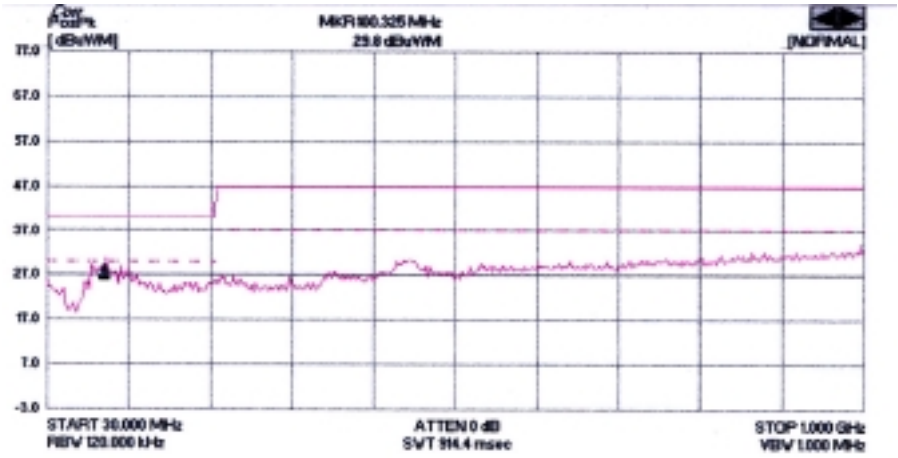


Figure 17. Radiated Emission, EN55022

The measured emission is remarkably free from peaks and shows more than 10-dB margin to the limits. This shows that the EMI-compliant design can be housed in a nonclosed metal box that has been designed with care.

EMI results depend on a number of factors that cannot be controlled in the chip set, but that are determined by the output filtering, power supply filtering and decoupling, PCB layout, the grounding scheme used in the chosen box, having ferrite beads on the wire, etc. Radiated and conducted emissions are often hard to control, but if care is taken during design and PCB layout, the task is reduced.

With the application example shown here as a guide, it should be a manageable task to do an EMI-compliant design.

7.2 Schematics

See Appendix A for schematics of the application example. Shown are the TAS5010 PCM-PWM modulator (U400) and two TAS5100 H-bridge power devices (U500 and U520).

This design shows an I^2S audio stream input to U400 (pins SDIN, SCLK, LRCLK and MCLK). The output is an AD mode PWM 3.3-V signal input to U500 (left channel) and U520 (right channel).

The TAS5010 uses an internal PLL circuit completed by external components R403, C401, and C400. The PLL power supply is AVDD2 and AVSS2. Note that AVSS2 is isolated from digital ground by the 1-Ω resistor R400. When laying out this circuit to build a PCB, it is recommended that a PLL ground island (AVSS2) be constructed under the PLL and oscillator section of the chip (pins 1-5 and pins 44-48).

TAS5010 control pins are DEM_EN, DEM_SEL, DBSPD, /MUTE, /RESET, /PDN, MOD2, MOD1, and MOD0. See the TAS5010 data sheet, literature number SLAS328, for more information.

The two output sections contain identical circuitry for left and right channels. This discussion focuses on the left channel. The TAS5100 (U500) requires some external components for dead-time control, power supply snubbing, demodulation filter, and EMI filters.

External resistors R501 and R502 accomplish dead-time control for the output PWM signals. For this design, the optimized values for these dead-time resistors are 13 kΩ.

Each TAS5100 has two half-bridges (A-side and B-side) that are shown connected in a full-bridge configuration. There is an identical power supply snubber circuit for each half-bridge. The A-side, left channel, snubber consists of L560, C505, and R504. The B-side, left channel, snubber consists of L561, C506, and R505. Note that inductors L560, L561, L562, and L563 are each a track in the PCB, 0,5 mm wide and 40 mm long.

The demodulation filter for the left channel consists of two inductors (L540 and L541) and a differential cap (C544). This low-pass filter rejects the switching frequency and other out-of-band components providing an analog signal to the speakers. Also shown are high-frequency bypass capacitors C545 and C546.

The EMI filter for the left side consists of R540 and C542 for the positive (+) terminal and R541, and C543 for the negative (–) terminal. These filters should be placed as close to the output terminals as possible with the routing tracks as short as possible. The output terminals to the speakers provide dc-coupled differential signals. This design is robust, offering protection against output shorts and overheating.

7.3 Recommended Closed-Loop Reset Configuration

Not shown in the schematics is the recommended closed-loop reset scheme for TAS50XX and TAS51XX devices. See Figure 18 for recommended circuitry. /SHUTDOWN goes low under several conditions. One of these is an overcurrent condition. If the system senses an over-current condition a delayed version of /SHUTDOWN causes the entire TDAA system to reset providing a graceful way to manage potential fault conditions. See the TAS5100 data sheet, literature number SLLS419 for more information on TAS5100 control and status signals.

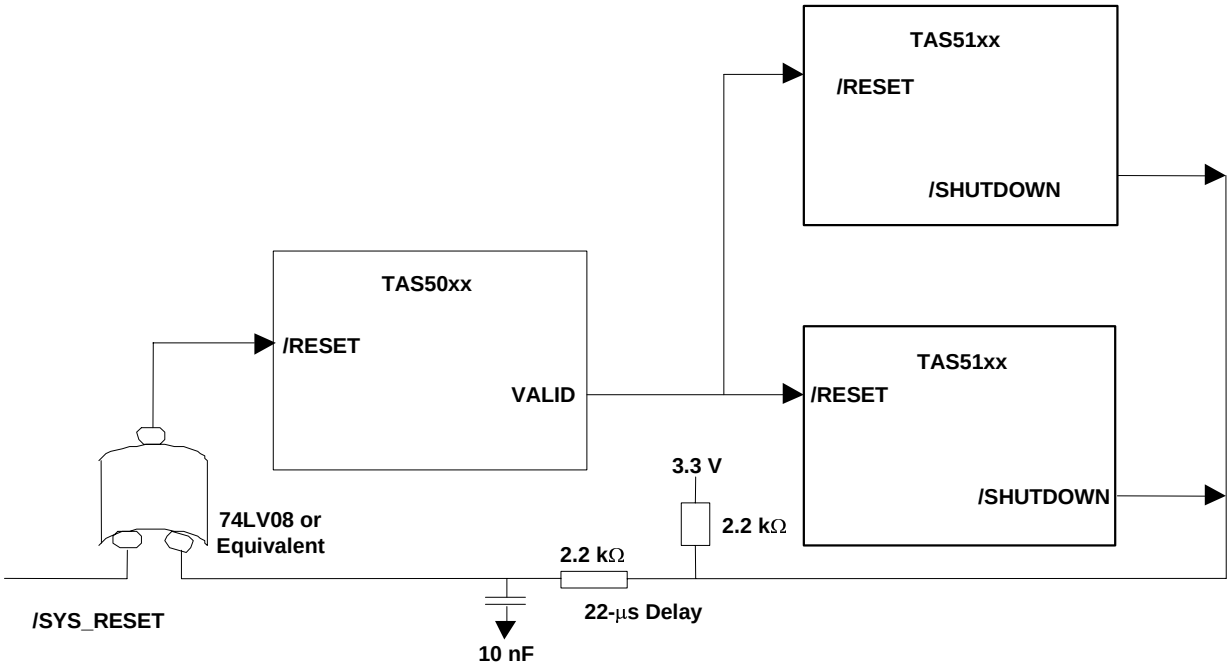


Figure 18. Recommended Closed-Loop Reset Configuration

7.4 Layout Considerations

Figure 19 shows an example implementation of this design. The TDAA circuitry is shown bordered in white. The actual dimensions of this section are approximately 2 1/2" X 2 1/4". Note the symmetry of the layout. The A-side and the B-side are symmetrical with respect to each other and each channel is also symmetrical with respect to each other. In general, track lengths are kept as short as possible with minimum inductance between each node. Three plated standoff holes that are ground potential are shown. These help to dissipate heat from the grounded power pad to the chassis. They also help in reducing EMI emissions. The power-supply snubber for the A-side is shown. Note that the inductor for this circuit is a PCB track (see *Schematics*). The demodulation filter and the high-frequency bypass capacitors are shown. Again note the compactness of the layout and the short PCB tracks. The power supply capacitors are shown between the demodulation filter and the output connectors. Finally, EMI filters are shown placed as close to the output connectors as possible.

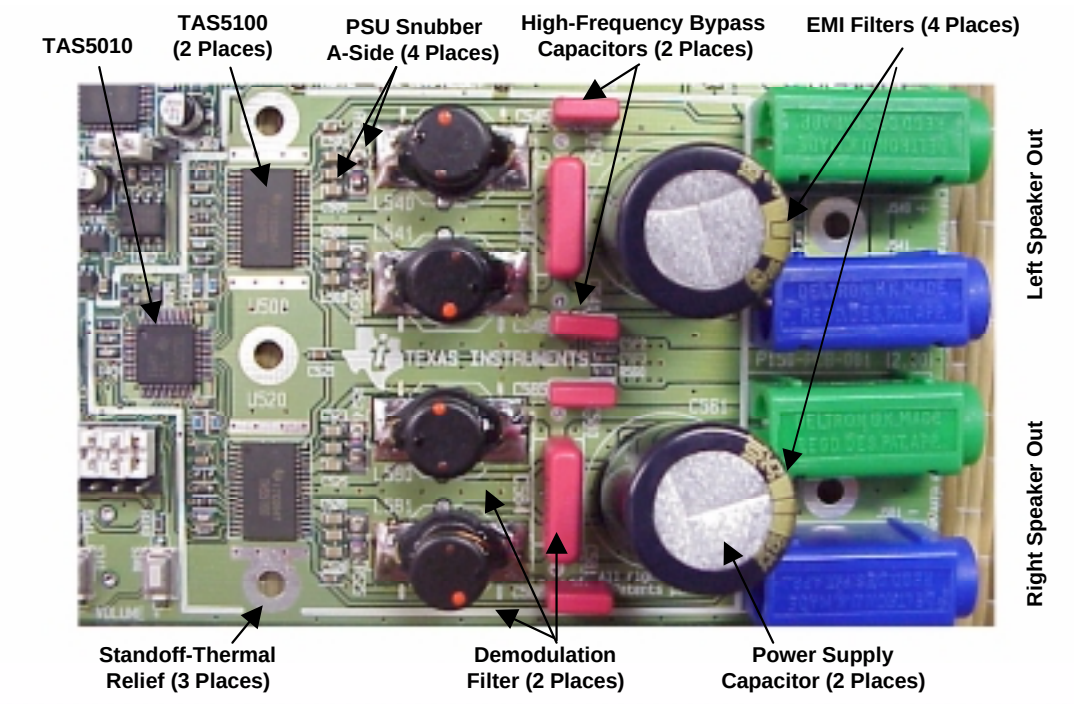


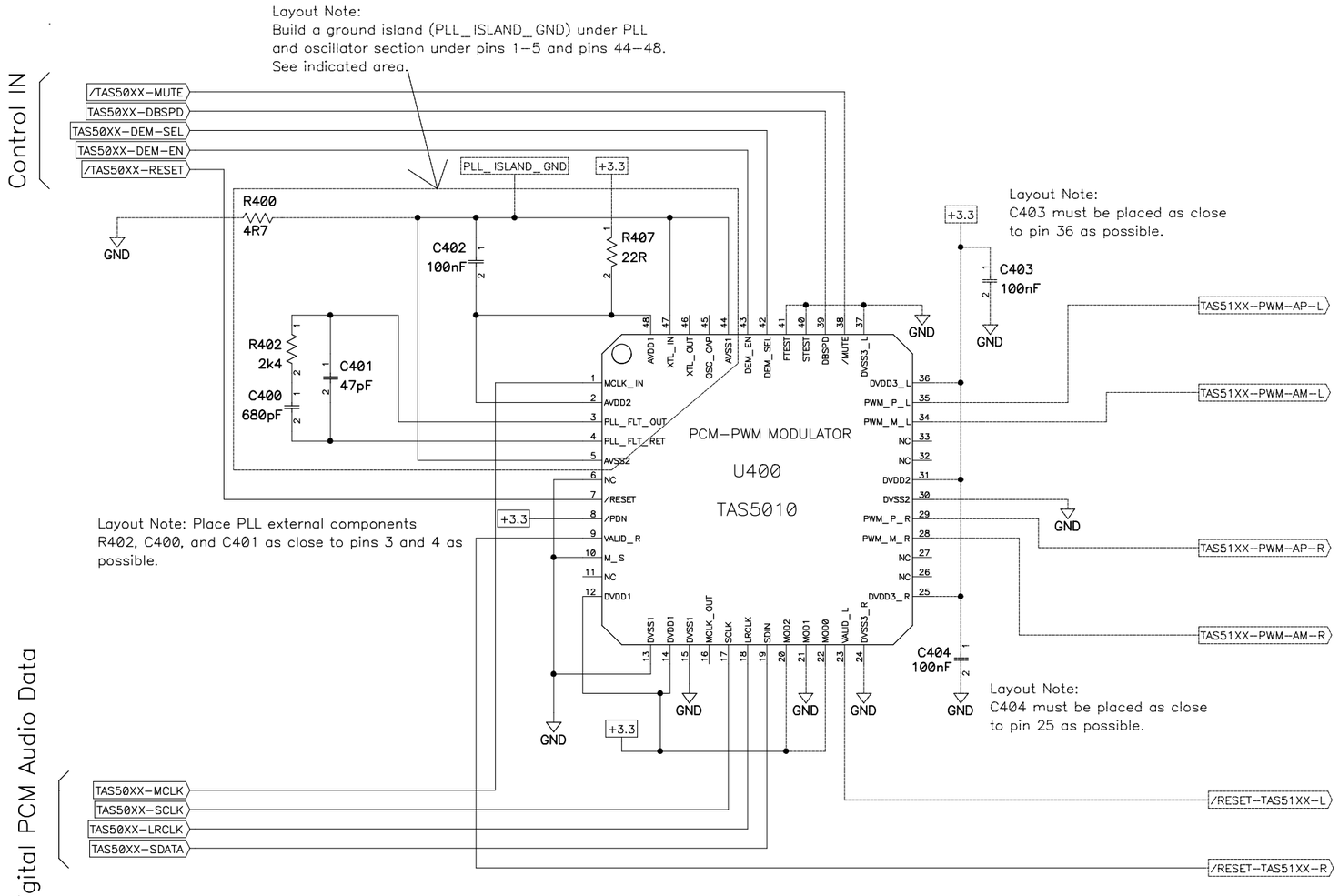
Figure 19. Application Example Layout

8 References

1. *Conversion of a PCM Signal into a UPWM Signal*, Australian Patent 721526
2. *Digital Audio Measurements*, application report, Texas Instruments Literature Number SLAA114
3. *TAS5000 Digital Audio PWM Processor*, data sheet, Texas Instruments Literature Number SLAS270
4. *TAS5100 Digital Audio PWM Power Output Stage*, data sheet, Texas Instruments Literature Number SLLS419
5. *TAS5001 Digital Audio PWM Processor*, data sheet, Texas Instruments Literature Number SLES009
6. *TAS5010 Digital Audio PWM Power Output Stage*, data sheet, Texas Instruments Literature Number SLAS328
7. *PowerPAD Thermally Enhanced Package*, application report, Texas Instruments Literature Number SLMA002
8. *TAS3001C Stereo Audio Digital Equalizer*, data manual, Texas Instruments Literature Number SLAS226

Appendix A

Appendix A. Application Example Schematics



Title	TDAA Application Example
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Filename	
Sheet	1 of 2

Layout Note:
EMI filter Resistor and Capacitor
placed close to the connector pins.

LEFT OUTPUT STAGE

U500
TAS5100

TAS51XX–PWM–AP–L
TAS51XX–PWM–AM–L
/TAS51XX–SHUTDOWN
+3.3
R500 10R
C500 100nF
C501 100nF
R501 13k
R502 13k
C502 100pF
R503 10R
/RESET–TAS51XX–L
TAS51XX–PWM–AP–L
TAS51XX–PWM–AM–L

PWM_AP, PWM_AM, /ERR1, /ERR0, /SHUTDOWN, DVDD, DVSS, DVSS, DVSS, VRFILT, BIASA, BIASB, /PWDN, /RESET, PWM_BM, PWM_BP

PVDDA2, LDROUTA, BOOTSTRAPA, PVDDA1, PVDDA1, OUTPUTA, OUTPUTA, PVSS, PVSS, OUTPUTB, OUTPUTB, PVDDB1, PVDDB1, BOOTSTRAPB, LDROUTB, PVDDB2

C503 100nF
C504 33nF
C505 200nF
R504 1R5
C506 200nF
R505 1R5
C507 33nF
C508 100nF
C509 33nF
VGATEDRV
PVDDA–L
PVDDB–L
PWM–OUTPUTA–L
PWM–OUTPUTB–L
GND

Layout Note:
Build a ground island below components
as shown.

RIGHT OUTPUT STAGE

U520
TAS5100

TAS51XX–PWM–AP–R
TAS51XX–PWM–AM–R
/TAS51XX–SHUTDOWN
+3.3
R520 10R
C520 100nF
C521 100nF
R521 13k
R522 13k
C522 100pF
R523 10R
/RESET–TAS51XX–R
TAS51XX–PWM–AP–R
TAS51XX–PWM–AM–R

PWM_AP, PWM_AM, /ERR1, /ERR0, /SHUTDOWN, DVDD, DVSS, DVSS, DVSS, VRFILT, BIASA, BIASB, /PWDN, /RESET, PWM_BM, PWM_BP

PVDDA2, LDROUTA, BOOTSTRAPA, PVDDA1, PVDDA1, OUTPUTA, OUTPUTA, PVSS, PVSS, OUTPUTB, OUTPUTB, PVDDB1, PVDDB1, BOOTSTRAPB, LDROUTB, PVDDB2

C523 100nF
C524 33nF
C525 200nF
R524 1R5
C526 200nF
R525 1R5
C527 33nF
C528 100nF
C529 33nF
C530 33nF
VGATEDRV
PVDDA–R
PVDDB–R
PWM–OUTPUTA–R
PWM–OUTPUTB–R
GND

DEMODULATION FILTER LEFT CHANNEL

L540 10uH
L541 10uH
C544 470nF
C545 150nF
C546 150nF
R540 1R
R541 1R
C542 10nF
C543 10nF
EMI Filter
R540 and C542
EMI Filter
R541 and C543
Green
4MM_PCB_SOCKET
J540
J541
Blue
SPEAKER OUTPUT LEFT CHANNEL

DEMODULATION FILTER RIGHT CHANNEL

L580 10uH
L581 10uH
C584 470nF
C585 150nF
C586 150nF
R580 1R
R581 1R
C582 10nF
C583 10nF
EMI Filter
R580 and C582
EMI Filter
R581 and C583
Green
4MM_PCB_SOCKET
J580
J581
Blue
SPEAKER OUTPUT RIGHT CHANNEL

POWER SUPPLY FILTER

Layout Note:
L560, L561, L562 and L563 are each a track in the PCB (0.5mm wide and 40mm long) yielding approximately a 50nH to 75nH inductor.

PVDDA–L
PVDDB–L
PVDDA–R
PVDDB–R
L560 50nH to 75nH
L561 50nH to 75 nH
L562 50nH – 75nH
L563 50nH to 75 nH
C560 1800uF
C561 1800uF
C562 1nF
C563 10nF
R560 1R
POWER–OUTPUT–STAGE
GND

Title	TDAA Application Example	
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