Dual-Output 8-Bit PWM DAC Using Low-Memory MSP430™ MCUs

TEXAS INSTRUMENTS

Introduction

Many applications, such as toys, musical tuners, function generators, and others require the generation of reference analog waveforms and signals. This is often done using a digital-to-analog converter, however with a few passive components, this can be achieved by utilizing pulse width modulation (PWM) signals. This report demonstrates how to generate time-variant and DC signals; however, it can be adapted to construct many other arbitrary signals using tables or counters, multiple programmable DC levels, or a combination. For supplemental reading, see *Using PWM Timer_B as a DAC Microcontrollers*. To get started, download project files and a code example demonstrating this functionality.

This example realizes an 8-bit DAC generating a 250-Hz sine wave, oversampled at 16x, and a DC signal. The sine wave is achieved by storing the sine samples in a lookup table, and updating the PWM duty cycle duration with the next sample after each PWM cycle. The PWM is output to an RC filter, which removes the higher-frequency signal components and reconstructs the sine wave. For this reason, it is best for the PWM frequency to be much higher than the desired sine frequency. To generate the DC, a constant duty cycle is maintained.

The target device, the MSP430FR2000 MCU, is a cost-effective device with 512 bytes of main memory. Larger MSP430™ devices can be substituted for more data storage or added functionality.

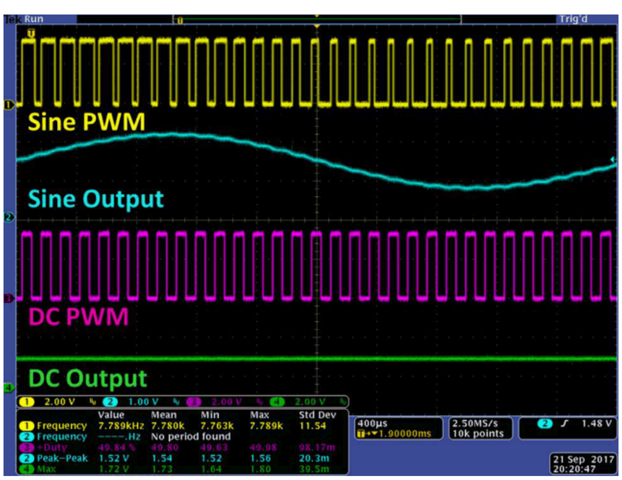

Figure 1. PWMs and Output

In Figure 1, the sine PWM duty cycle can be seen changing after each PWM period, whereas the DC duty cycle is not. The sine and DC waves are seen at the output of the RC filters.

Implementation

The resolution of the DAC is determined by the timer count length ($2^8 = 256$). The sampling rate, or PWM frequency, can be found by multiplying the sine frequency by the number of samples per sine cycle, which gives 8 kHz.

$$32_{\text{Samples}} \times 250\ \text{Hz} = 8\ \text{kHz} \quad (1)$$

An easy way to think about this relationship is that the capacitor is essentially averaging the output samples over time. So the sampling rate is the output sample speed required to construct a 250Hz periodic signal with 32 samples per cycle.

The PWM clock frequency is then found by multiplying the sampling frequency by the number of timer counts, which gives 2.048 MHz. To achieve this, the digitally controlled oscillator (DCO) has been set to 16 MHz, with a master clock (MCLK) divider of 4, and a subsystem master clock (SMCLK) divider of 2, (16 MHz / 4 / 2 = 2 MHz). SMCLK then sources Timer_B, which has CCR0 = 256.

Resolution, PWM frequency, and PWM clock frequency can also be shown in the relation:

$$f_{clock} = f_{PWM} \times 2^{nBits}$$

where

- nBits = the bit resolution of the DAC (2)

The CCR0 interrupt is enabled and, each time it fires, the ISR updates the PWM duty cycle, stored in CCR1. This is done by incrementing the counter variable to point within a 32-element sine wave array. CCR2 is loaded with a constant PWM duty cycle to generate the DC signal. CCR1 and CCR2 are configured for pins P1.6/TB0.1 and P1.7/TB0.2. Alternatively, P2.0 and P2.1 could be used. Both CCR output modes are set to reset/set. In this mode, each output is reset when the counter reaches the respective CCRx value and is set when the counter reaches the CCR0 value. This provides positive pulses equivalent to the value in CCRx on each respective output.

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By outputting the sine PWM to a 2-pole stacked RC filter, the sine wave is reconstructed and the PWM switching is filtered out. The R and C values can be determined by Equation 3.

$$f_C = \frac{1}{2\pi RC}$$

where

- R1C1 = R2C2 = RC (3)

The filter cutoff (here 795 Hz) is chosen to be sufficiently higher than the bandwidth edge to reduce attenuation, but lower than the frequency of the PWM signal to filter out its switching. This filter gives better response when R2>>R1, due to the effect of the voltage divider that is present. The second order passive filter topology was chosen for its simplicity, however necessitates a higher sampling frequency than if a higher order filter was used.

The filter for the DC signal is simply used for charge storage; thus, a single-pole filter is implemented.

This solution uses an MSP430FR2000 MCU and external resistors and capacitors to build the RC filter. The MSP430FR2000 device was used with the MSP-TS430PW20 target development board and connected as shown in Figure 2.

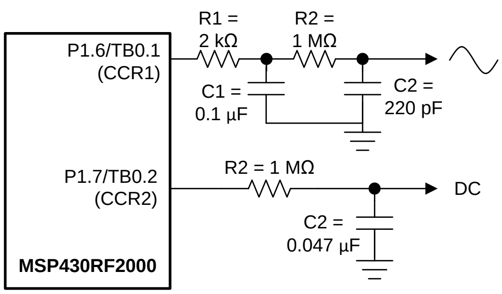

Figure 2. Output Filter Diagram

Performance

To run the demo, connect the hardware as previously described, load the code into the device, allow the device to run and end the debug session. Connect P1.6, P1.7, and the filter outputs to an oscilloscope or analog-capable logic analyzer to observe the signals (see Figure 3).

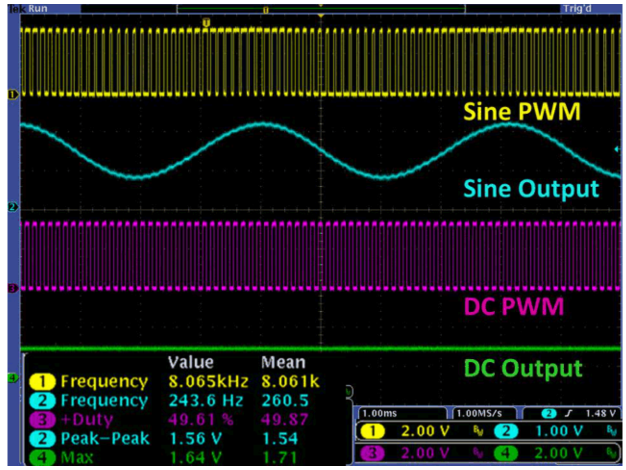

Figure 3. C2 = 220 pF, 1.64 VDC, 50% PWM

The output can be cleaned up by increasing the order of the filter, where the attenuation at the cutoff point of an n^th^-order filter can be found by Equation 4.

$$\frac{V_{out}}{V_{in}} = \left(\frac{1}{\sqrt{2}}\right)^n \quad (4)$$

or, by tuning the cutoff point further away from the PWM frequency, achieved here by increasing C2 to 420 pF (see Figure 4). However, the criterion for the previous f_C relation is violated; therefore the frequency (549 Hz in this example) is now obtained by Equation 5.

$$f_C = \frac{1}{2\pi\sqrt{R1C1R2C2}} \quad (5)$$

Additionally, the DC level can be changed by adjusting the duty cycle of the DC PWM (see Figure 3 and Figure 4). These values are directly proportional (attenuation may need to be accounted for depending on filter design) and follow the relationship:

$$V_{DC} = D \times V_{CC}$$

where

- D = PWM duty cycle (6)

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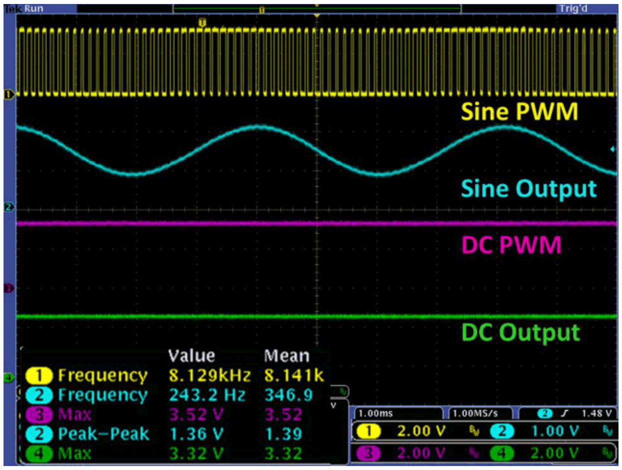

Figure 4. C2 = 420 pF, 3.32 VDC, 100% PWM

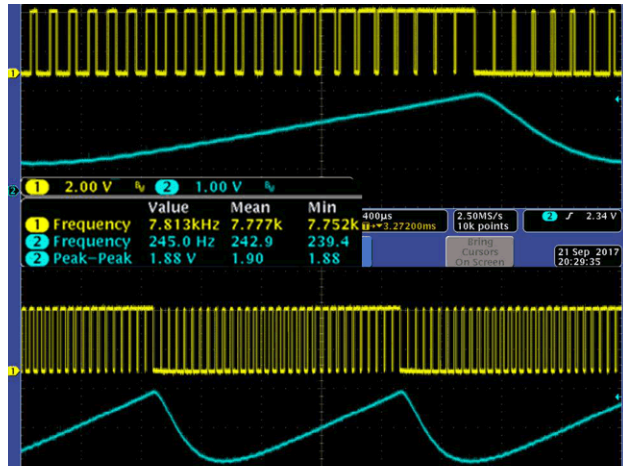

Figure 5. Output Ramp (Top Zoomed)

Furthermore, the DC and time-variant signals can be summed using a summing amplifier to achieve an offset. A simple up or up-down counter can be implemented to generate a ramp or triangle wave (see code and Figure 5). These topics are covered further in *Using PWM Timer_B as a DAC Microcontrollers*; however, the ISR to achieve a ramp and the resulting waveform are included below.

```
/**
 * TimerB0 Interrupt Service Routine
 **/
#pragma vector=TIMER0_B0_VECTOR
__interrupt void TIMER0_B0_ISR(void)
{
    //Increment PWM duty cycle in steps of 8
    //To adjust frequency, change step size
    dutyCycle+=8;
    // Set CCR1 using a 256 count bit mask
    TB0CCR1 = dutyCycle & 0x0FF;
}
```

Presumably, many other arbitrary waveforms can be reconstructed using the methods above, provided an oversampled table of the signal has been constructed. If the sample table exceeds 500 bytes, other MSP430 MCUs are available with larger memory sizes.

Device Recommendations

The device used in this example is part of the MSP430 Value Line Sensing portfolio of low-cost MCUs, designed for sensing and measurement applications. This example can be used with the devices shown in Table 1 with minimal code changes. For more information on the entire Value Line Sensing MCU portfolio, visit www.ti.com/MSP430ValueLine.

Table 1. Device Recommendations

Part Number	Key Features
MSP430FR2000	0.5KB FRAM, 0.5KB RAM, eComp
MSP430FR2100	1KB FRAM, 0.5KB RAM, 10-bit ADC, eComp
MSP430FR2110	2KB FRAM, 1KB RAM, 10-bit ADC, eComp
MSP430FR2111	3.75KB FRAM, 1KB RAM, 10-bit ADC, eComp

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